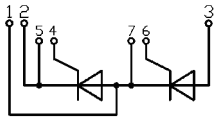
Double Thyristor Module For Phase Control MTx-125-28-F

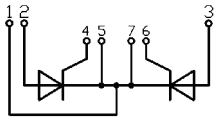
Electrically isolated base plate
Industrial standard package
Simplified mechanical design, rapid assembly
Pressure contact

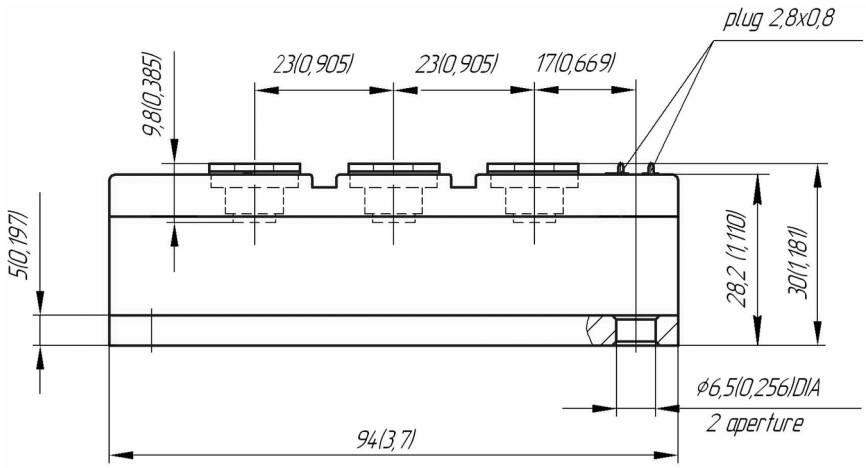
Mean on-state current	I_{TAV}	125 A
Repetitive peak off-state voltage	V_{DRM}	2400...2800 V
Repetitive peak reverse voltage	V_{RRM}	
Turn-off time	t_q	250 µs

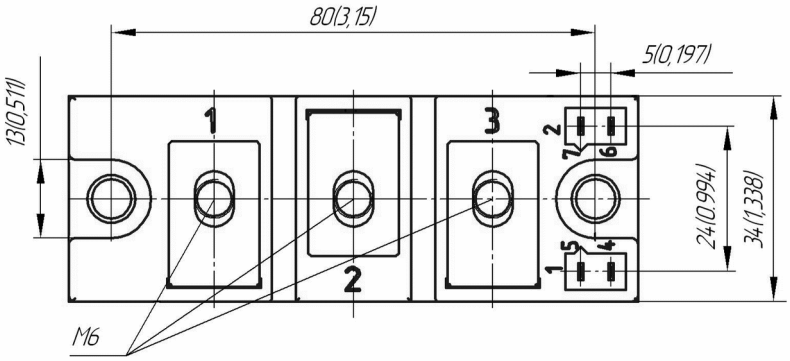
V_{DRM}, V_{RRM}, V	2400	2600	2800
Voltage code	24	26	28
T_j, °C	–40...+125		

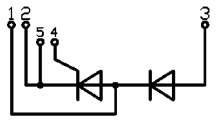
MT3 **MT4**

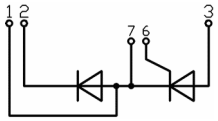


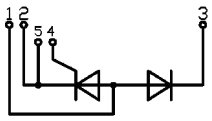












MT/D3 **MD/T3** **MT/D5**

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current	A	125 148	T_c= 92 °C; T_c= 85 °C; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	196	T_c= 92 °C; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	3.8 4.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			4.0 4.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor	$A^2s\cdot10^3$	70 100	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			60 80	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2400...2800	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2500...2900	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6\cdot V_{DRM}$ $0.6\cdot V_{RRM}$	T_j=$T_{j\,max}$; Gate open	
TRIGGERING					
I_{FGM}	Peak forward gate current	A	5	T_j=$T_{j\,max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	3	T_j=$T_{j\,max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	800	T_j=$T_{j\,max}$; V_D=$0.67\cdot V_{DRM}$; I_{TM}=840 A; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs	
THERMAL					
T_{stg}	Storage temperature	°C	–40...+50		
T_j	Operating junction temperature	°C	–40...+125		
$T_{c\,op}$	Operating temperature	°C	–40...+125		
MECHANICAL					
a	Acceleration under vibration	m/s^2	50		

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.80	T_j=25 °C; I_{TM}=500 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.246	T_j=$T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance, max	mΩ	0.915		
I_L	Latching current, max	mA	500	T_j=25 °C; V_D=12 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs	
I_H	Holding current, max	mA	250	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	40 2.50	T_j=$T_{j\,max}$ T_j= 25 °C	V_D=V_{DRM}; V_R=V_{RRM}
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1], min	V/µs	200, 320, 500, 1000, 1600, 2000, 2500	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	T_j= $T_{j\,min}$ T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	400 250 150	T_j= $T_{j\,min}$ T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.45	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	35.00		
SWITCHING					
t_{gd}	Delay time, max	µs	0.90	T_j=25 °C; V_D=1500 V; I_{TM}=I_{TAV}; di/dt=200 A/µs; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs	
t_{gt}	Turn-on time, max	µs	3.00		
t_q	Turn-off time[2], max	µs	250	dv_D/dt=50 V/µs; T_j=$T_{j\,max}$; I_{TM}=I_{TAV}; di_R/dt=-10 A/µs; V_R=100V; V_D=0.67 V_{DRM};	
Q_{rr}	Recovered charge, max	µC	1080	T_j=$T_{j\,max}$; I_{TM}=I_{TAV}; di_R/dt=-10 A/µs; V_R=100 V	
t_{rr}	Reverse recovery time, max	µs	24		
I_{rr}	Reverse recovery current, max	A	90		
THERMAL					
R_{thjc}	Thermal resistance, junction to case				
	per module	°C/W	0.0850	180° half-sine wave, 50 Hz	
	per arm	°C/W	0.1700		
	per module	°C/W	0.0800	DC	
	per arm	°C/W	0.1600		
R_{thch}	Thermal resistance, case to heatsink				
	per module	°C/W	0.0300		
	per arm	°C/W	0.0600		
INSULATION					
V_{ISOL}	Insulation test voltage	kV	3.00	Sine wave, 50 Hz; RMS	t=60 sec
			3.60		t=1 sec
MECHANICAL					
M_1	Mounting torque (M6)[3]	Nm	6.00	Tolerance ± 15%	
M_2	Terminal connection torque (M6)[3]	Nm	6.00	Tolerance ± 15%	
m	Weight, max	g	350		

PART NUMBERING GUIDE

MT	3	-	125	-	28	-	A2	M2	-	F	-	N
1	2		3		4		5	6		7		8

1. Thyristor module (MT)
   Thyristor – Diode module (MT/D)
   Diode – Thyristor module (MD/T)
2. Circuit Schematic:
3. Average On-state Current, A
4. Voltage Code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time (dv_D/dt=50 V/μs)
7. Package Type (M.F)
8. Ambient Conditions:
   N – Normal

NOTES

1) Critical rate of rise of off-state voltage

Symbol of Group	P2	K2	E2	A2	T1	P1	M1
$(dv_D/dt)_{crit}$, V/μs	200	320	500	1000	1600	2000	2500

2) Turn-off time (dv_D/dt=50 V/μs)

Symbol of group	M2
t_q, μs	250

3) The screws must be lubricated

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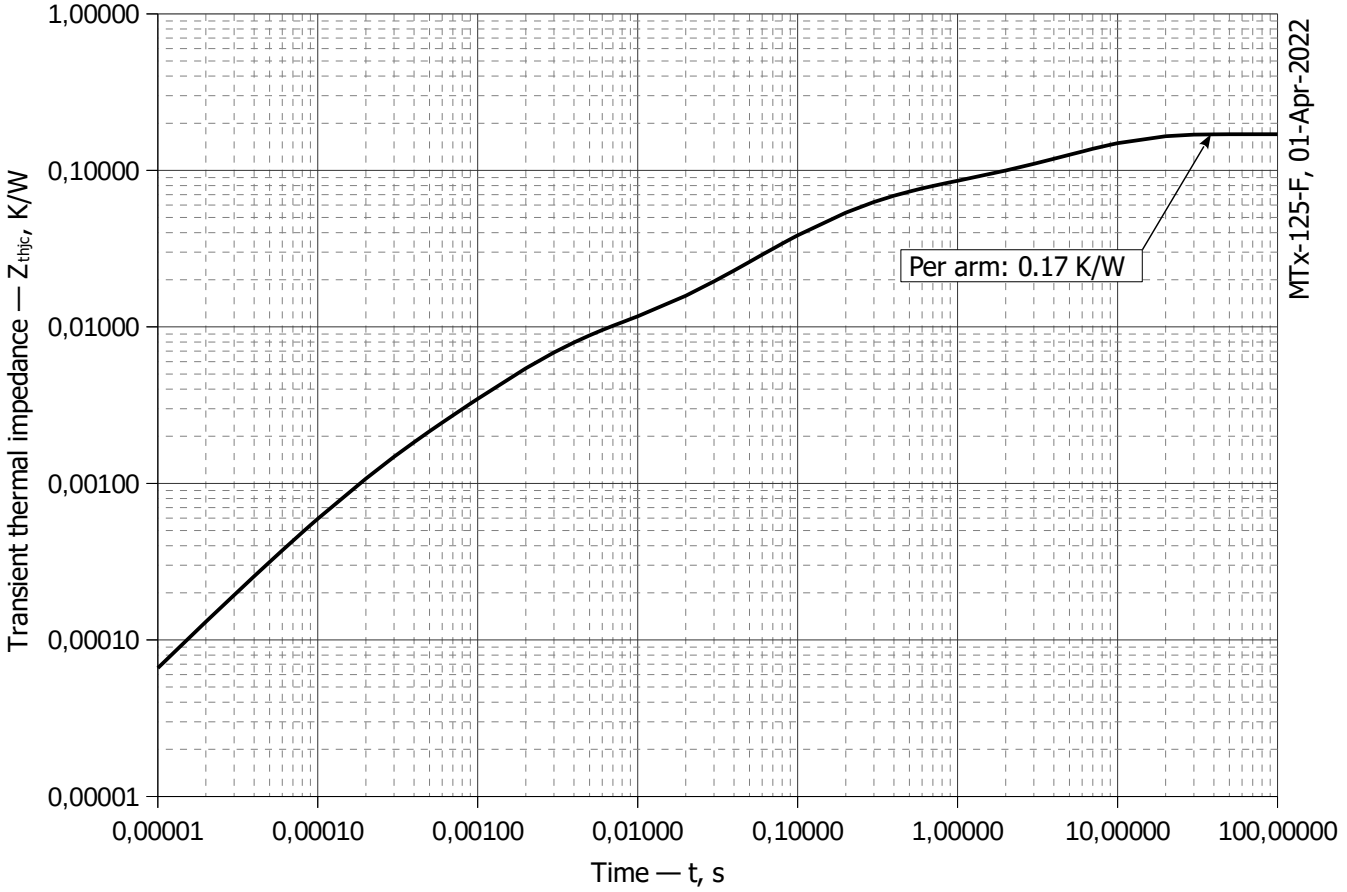

Fig 1 – Transient thermal impedance Z_{thjc} vs. time t

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

Z_{thjc} = Thermal resistance at time t.

R_i = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

i	1	2	3	4	5	6
R_i, K/W	0.0007228424	0.0066399867	0.0153862565	0.0389709604	0.0142906115	0.09398934
τ_i, s	0.0002111	0.002366	0.06905	0.1909	0.6646	6.64

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 1)

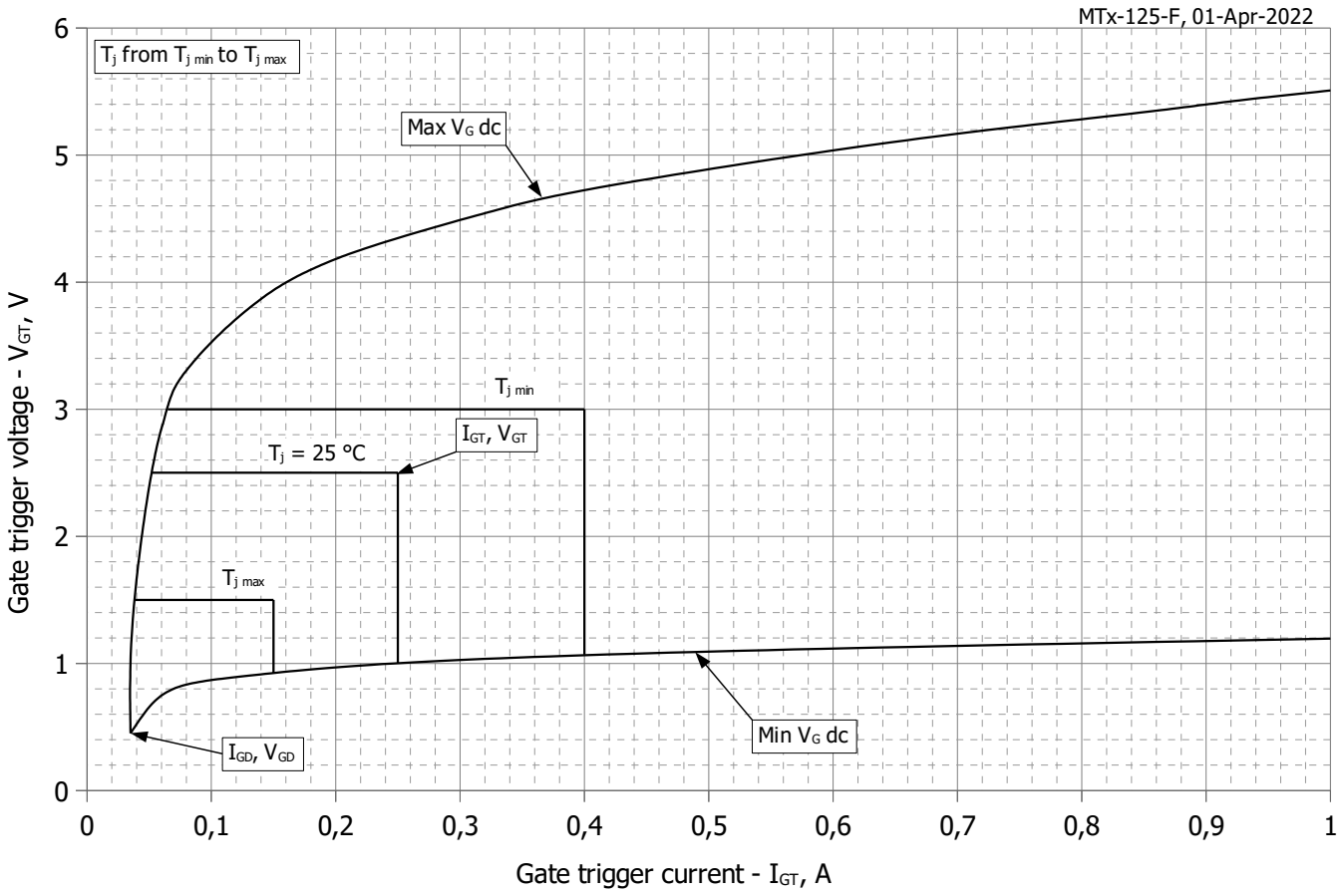

Fig 2 – Gate characteristics – Trigger limits

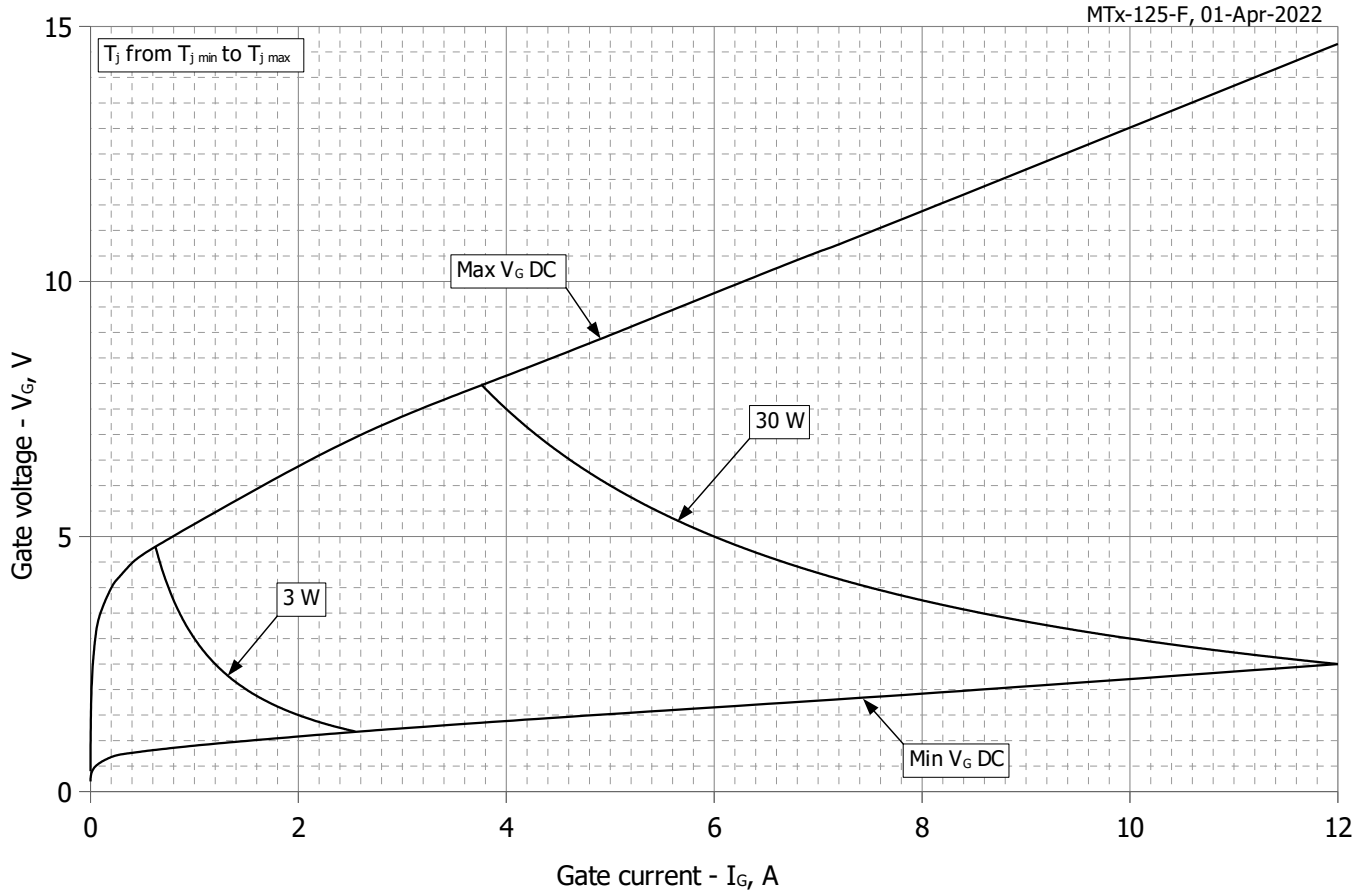

Fig 3 - Gate characteristics – Power curves

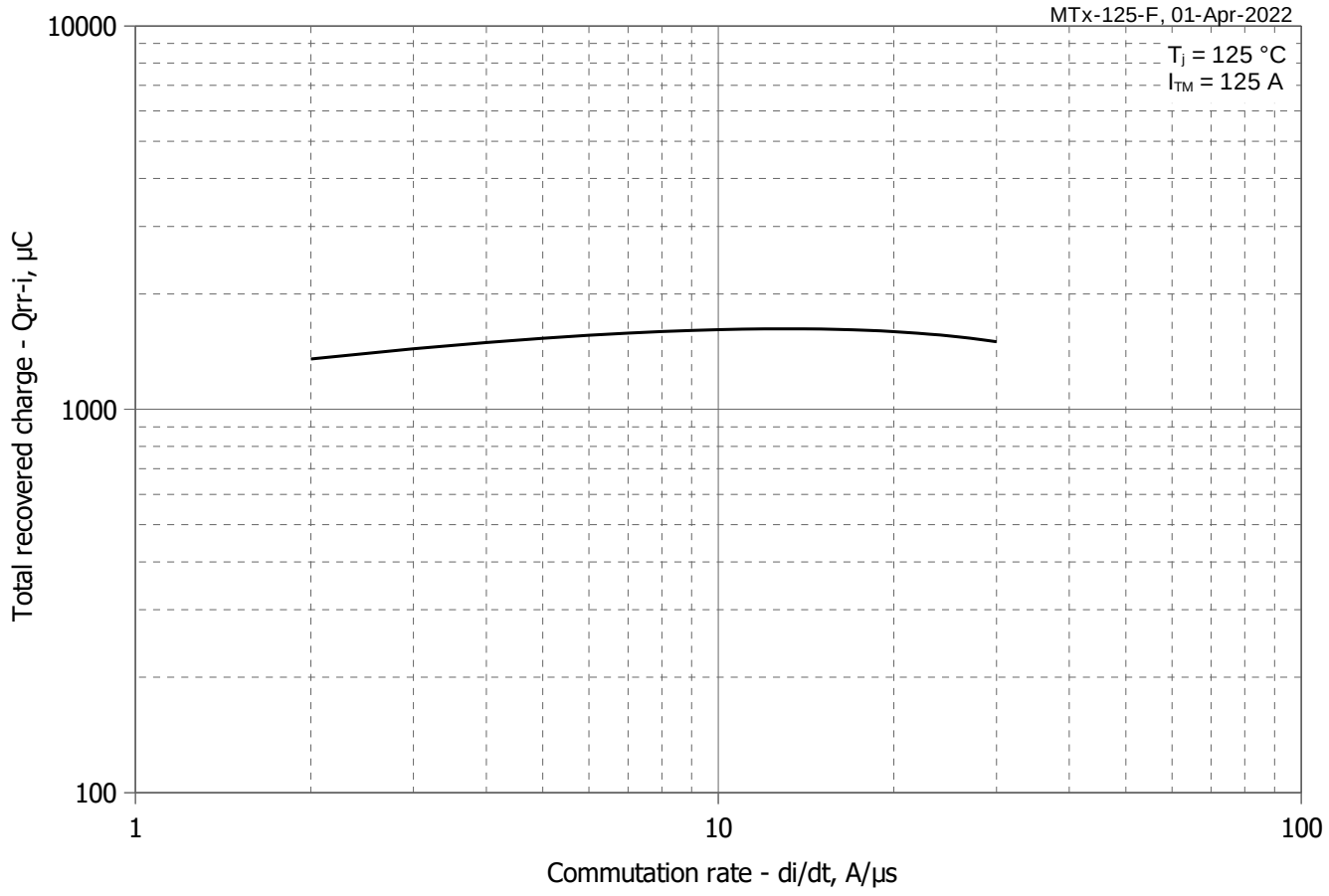

Fig 4 – Maximum recovered charge Q_{rr-i} (integral) vs. commutation rate di_R/dt

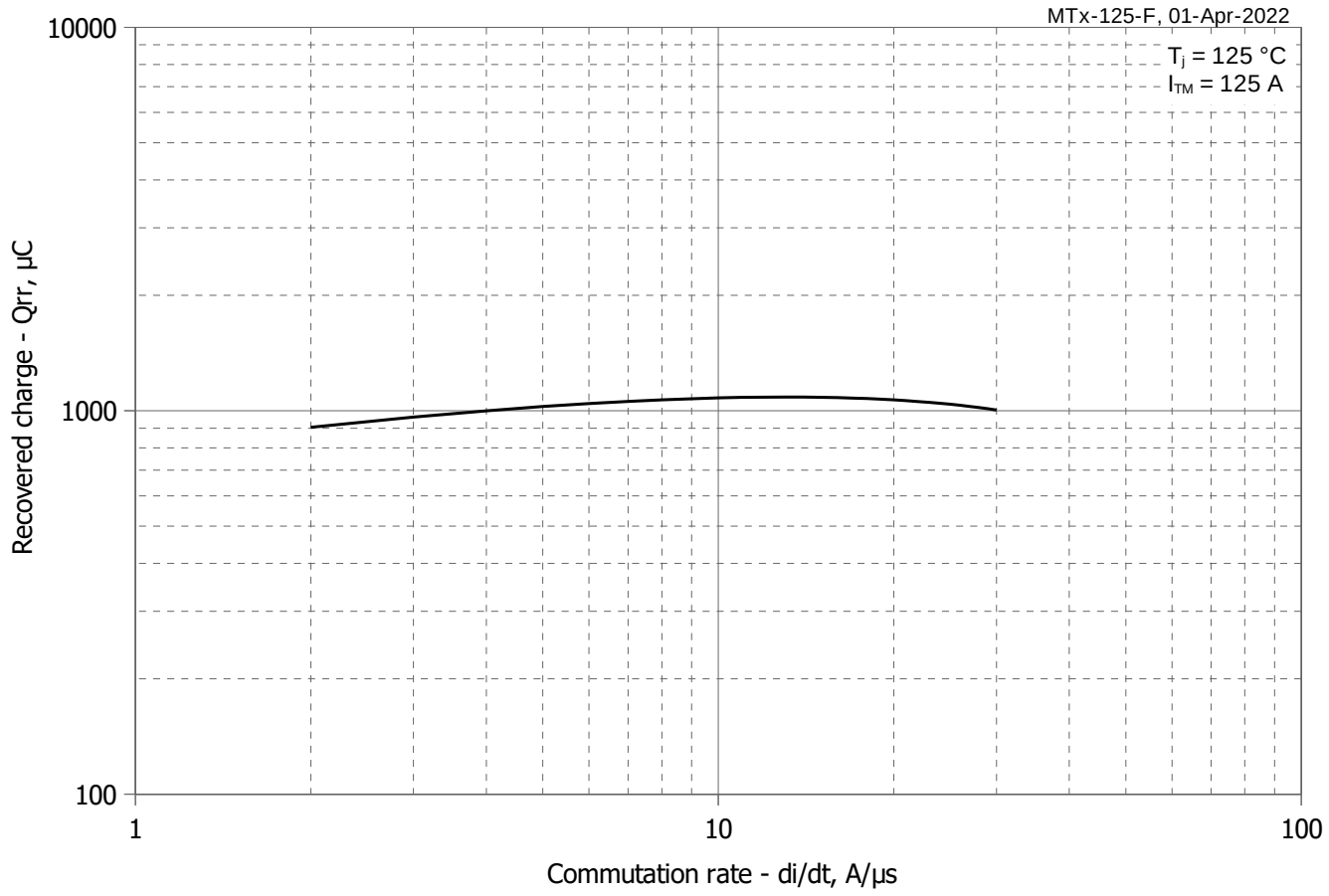

Fig 5 – Maximum recovered charge Q_{rr} vs. commutation rate di_R/dt (25% chord)

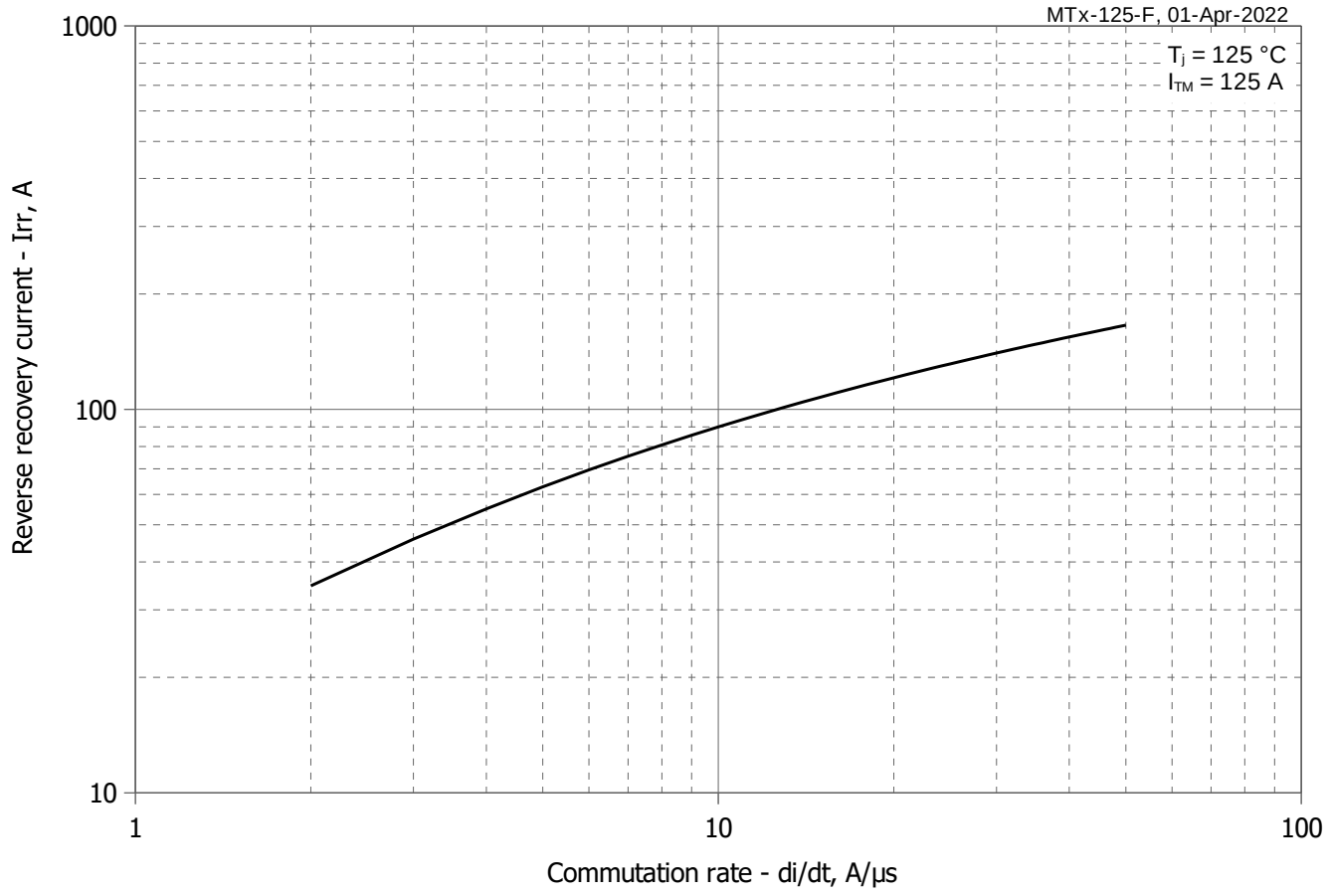

Fig 6 – Maximum reverse recovery current I_{rr} vs. commutation rate di_R/dt

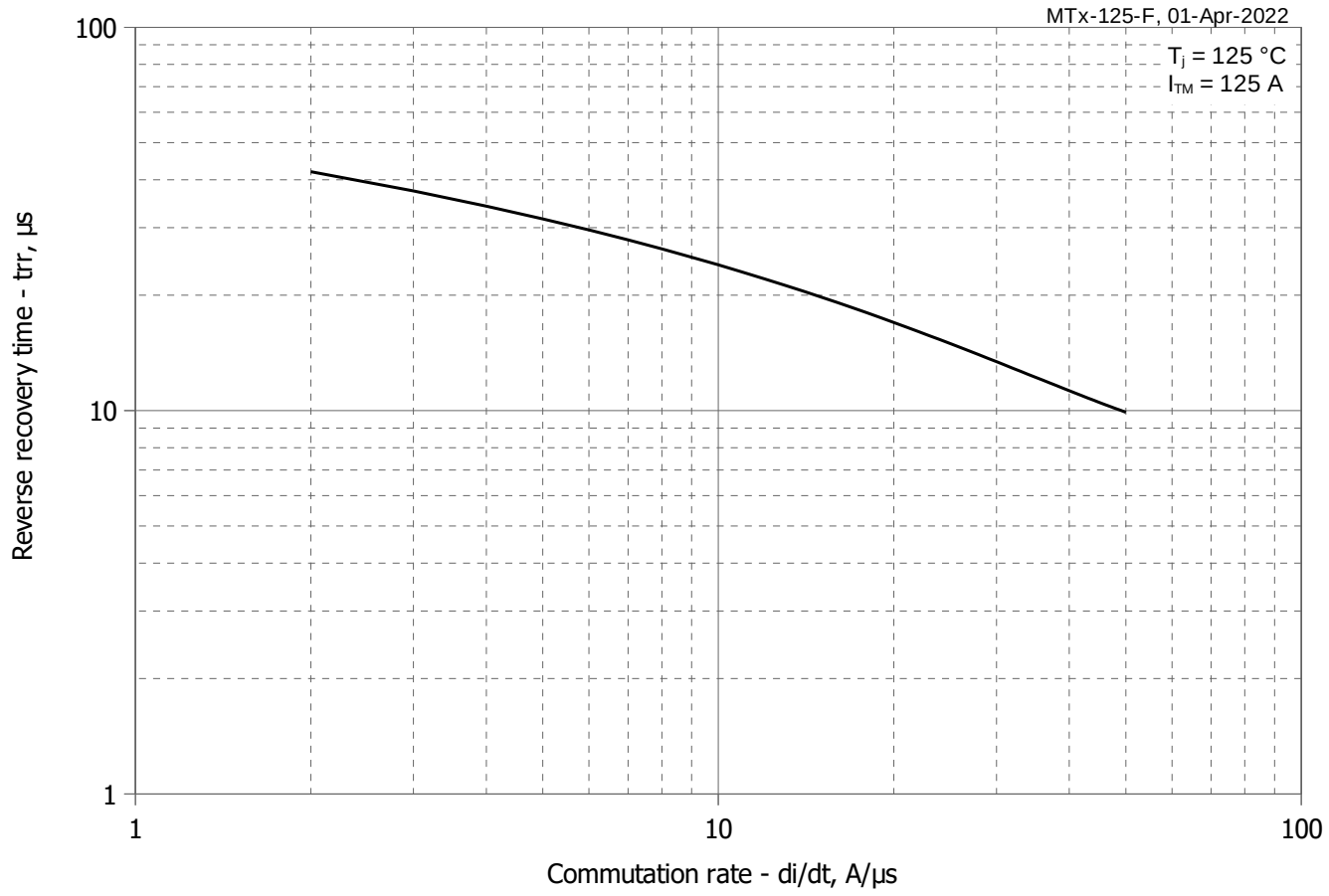

Fig 7 – Maximum recovery time t_{rr} vs. commutation rate di_R/dt (25% chord)

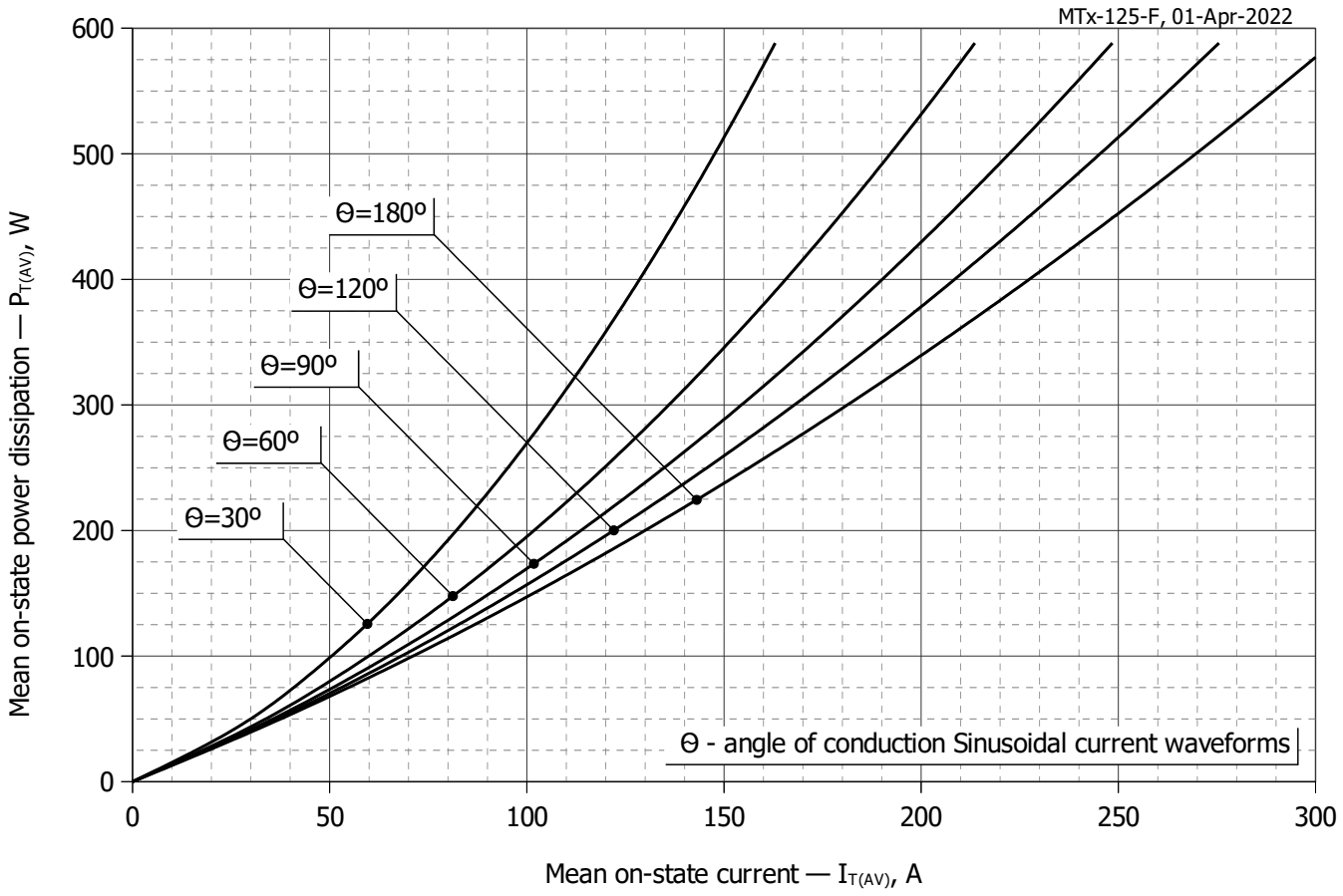

Fig. 8 - Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for sinusoidal current waveforms at different conduction angles (f=50Hz)

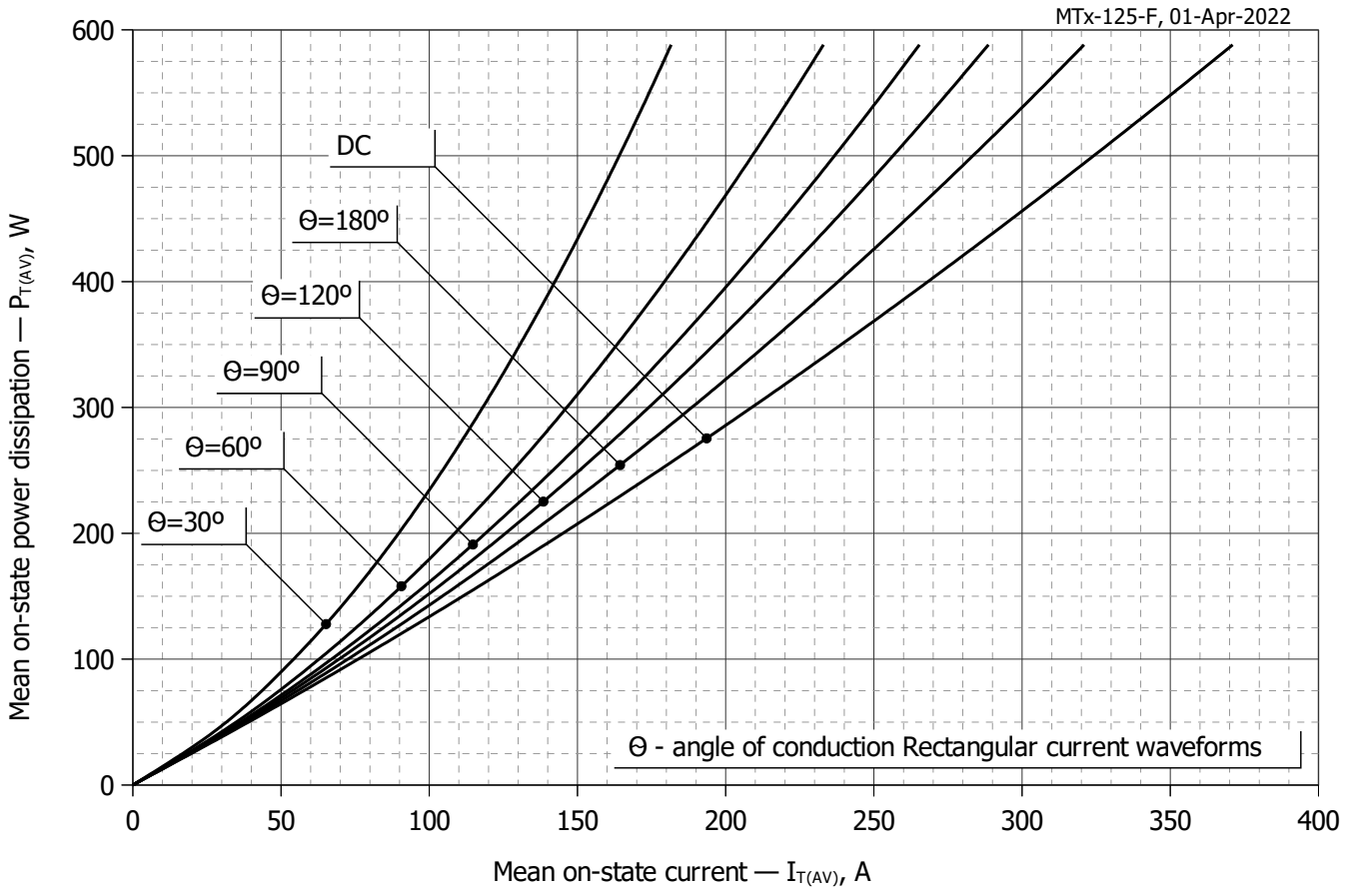

Fig. 9 – Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for rectangular current waveforms at different conduction angles and for DC (f=50Hz)

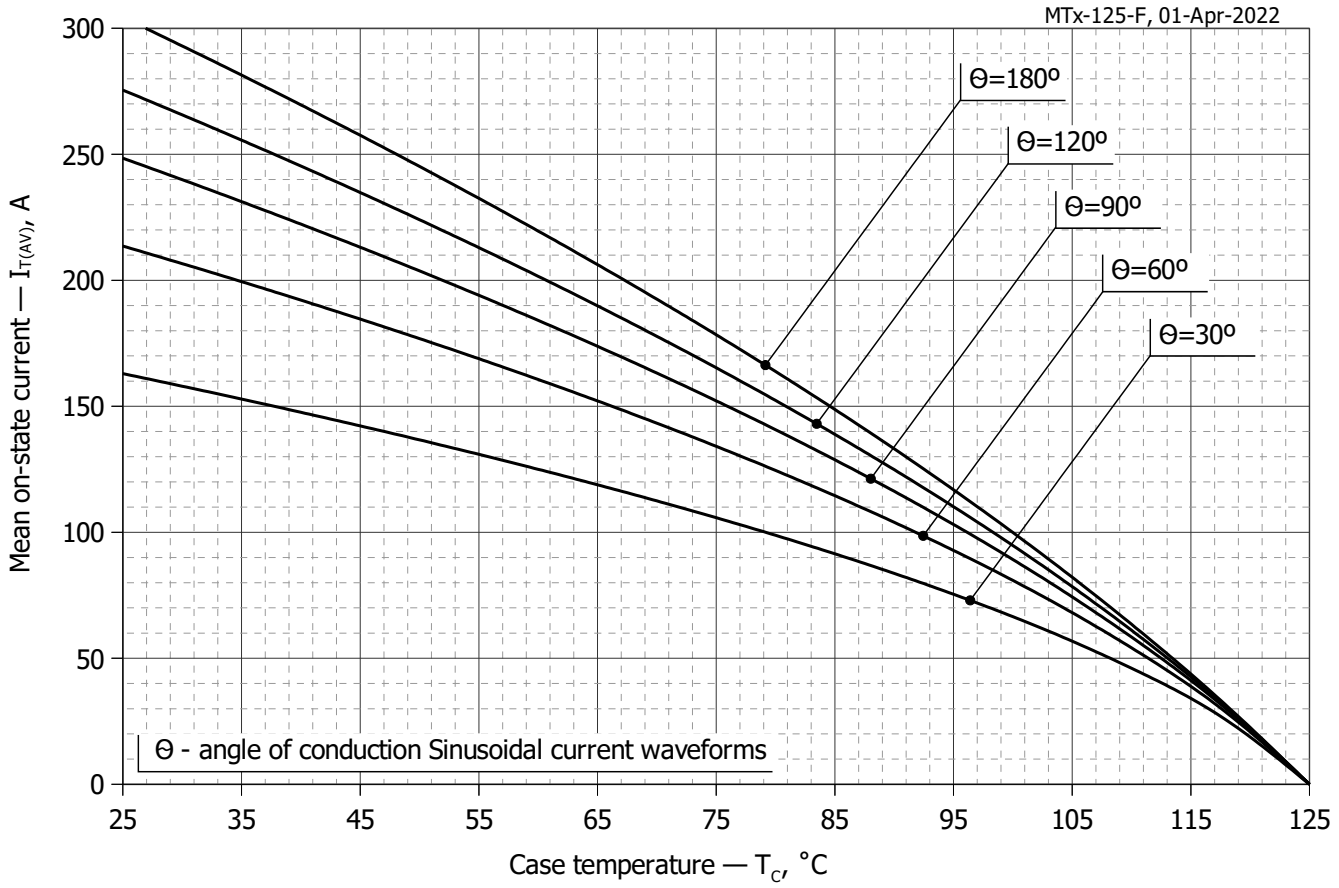

Fig. 10 – Mean on-state current I_{TAV} vs. case temperature T_C for sinusoidal current waveforms at different conduction angles (f=50Hz)

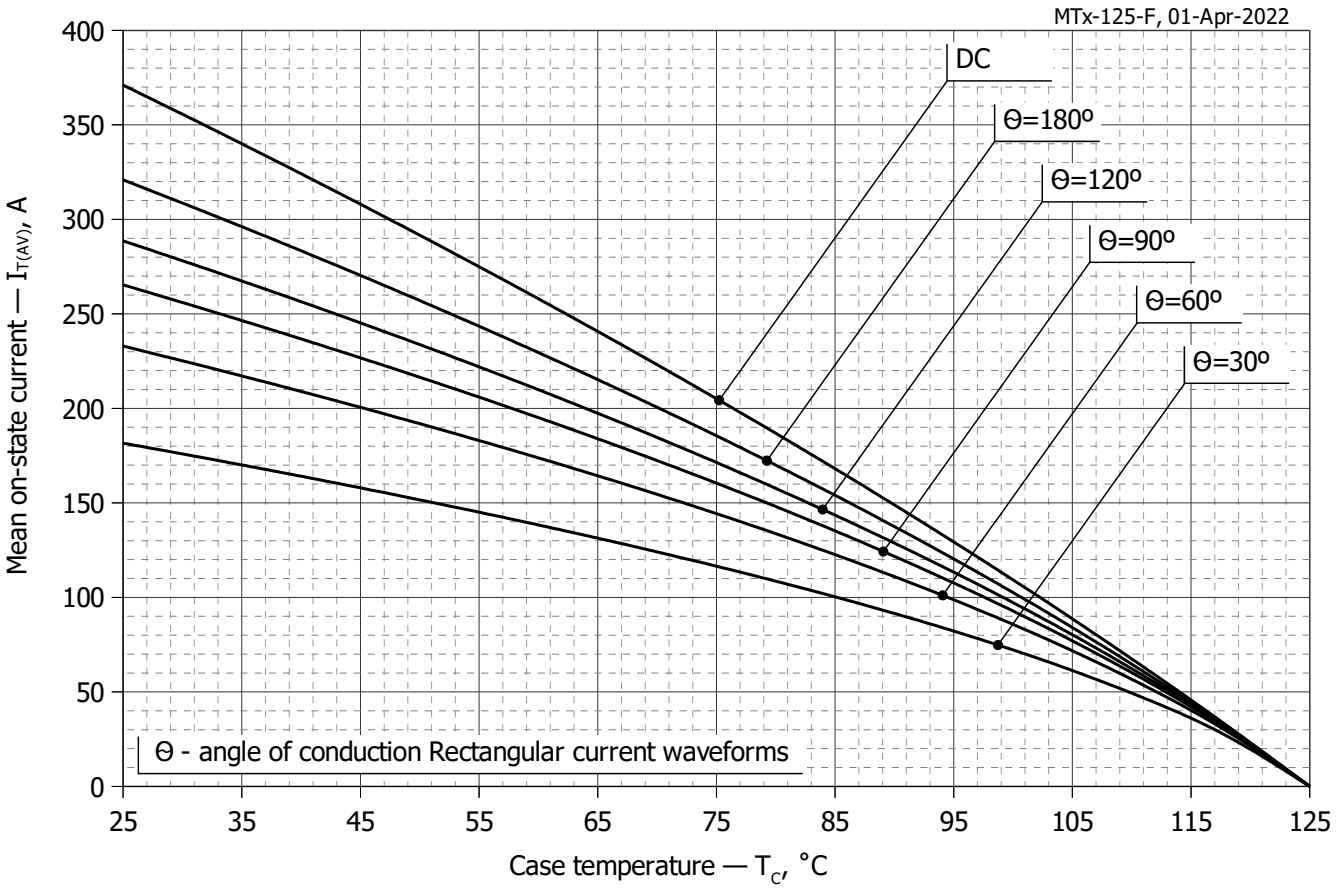

Fig. 11 - Mean on-state current I_{TAV} vs. case temperature T_C for rectangular current waveforms at different conduction angles and for DC (f=50Hz)

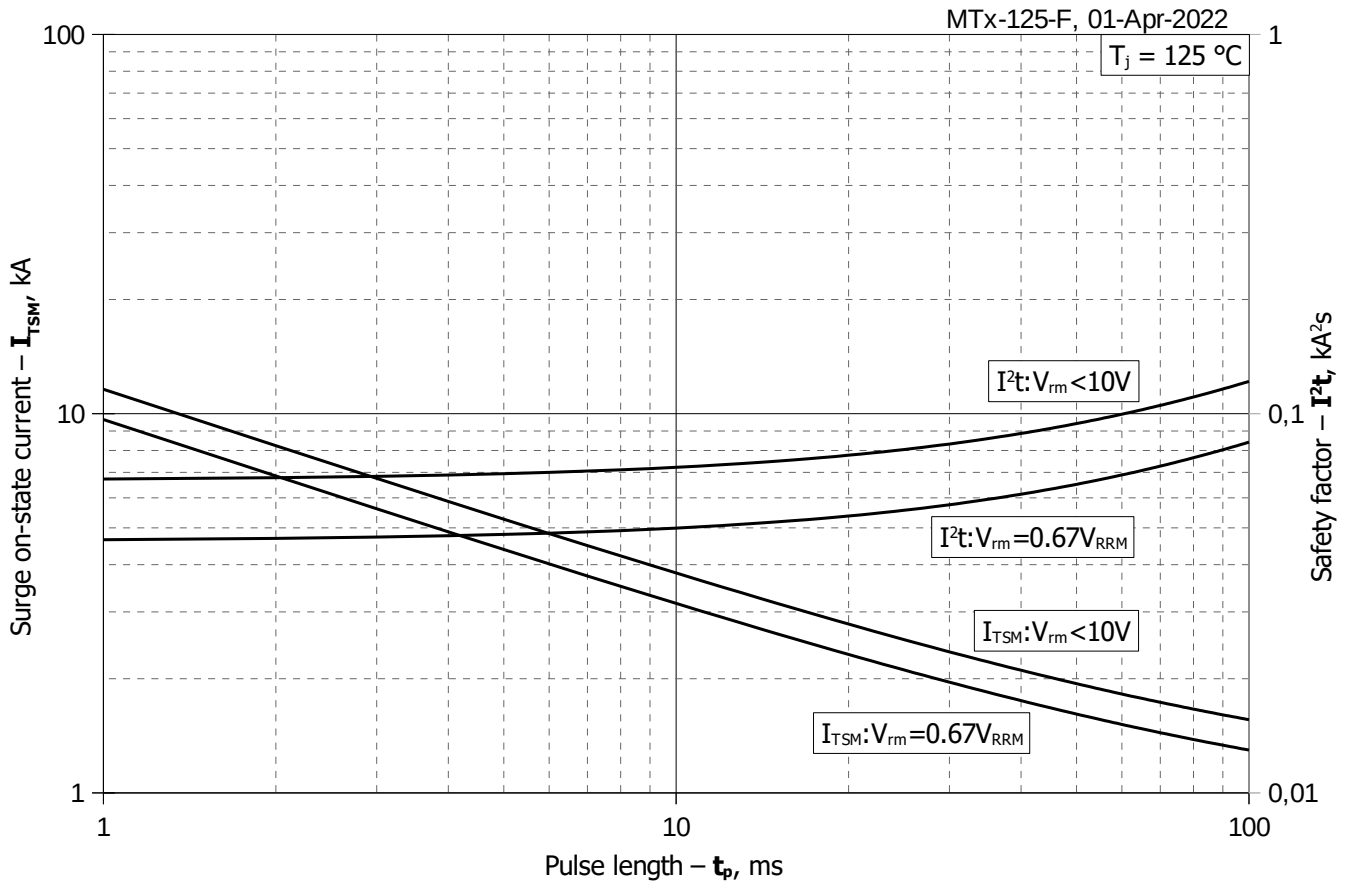

Fig. 12 – Maximum surge on-state current I_{TSM} and safety factor I^2t vs. pulse length t_p

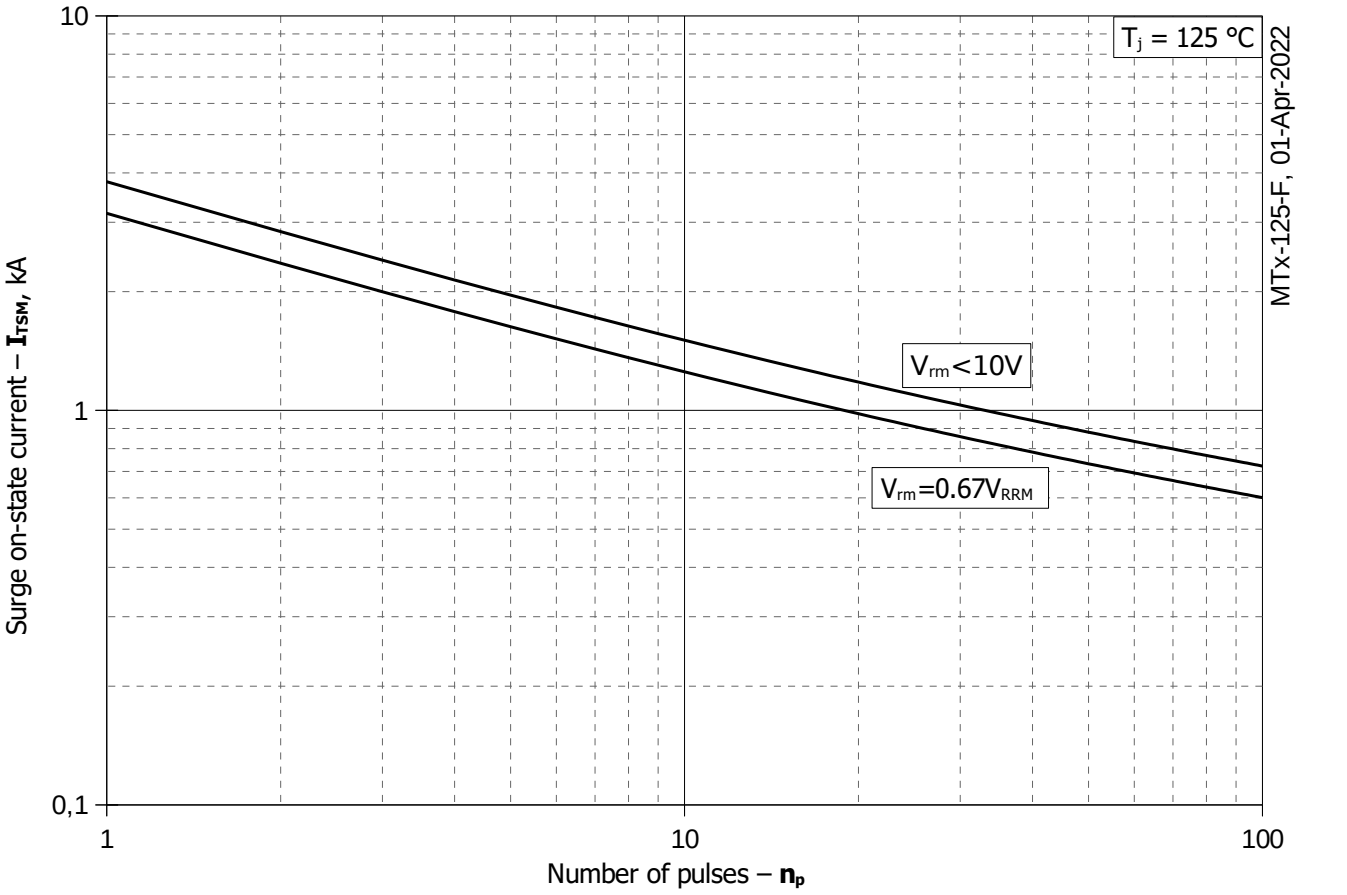

Fig. 13 - Maximum surge on-state current I_{TSM} vs. number of pulses n_p