



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor
Type T163-1250-44

Maximum allowable mean on-state current		I _{TAV}		1250 A	
Repetitive peak off-state voltage		V _{DRM}		3800...4400 V	
Repetitive peak reverse voltage		V _{RRM}			
Turn-off time		t _q		630 μs	
V _{DRM} , V _{RRM} , V	3800	4000	4200	4400	
Voltage code	38	40	42	44	
T _j , °C	-60...+125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current	A	1250 1838 2260	$T_c=102\text{ }^{\circ}\text{C}$, Double side cooled $T_c=85\text{ }^{\circ}\text{C}$, Double side cooled $T_c=70\text{ }^{\circ}\text{C}$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	1963	$T_c=102\text{ }^{\circ}\text{C}$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	26.0 30.0	$T_j=T_{j\max}$ $T_j=25\text{ }^{\circ}\text{C}$	180° half-sine wave; $t_p=10\text{ ms}$; single pulse; $V_D=V_R=0\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$
			27.0 31.0	$T_j=T_{j\max}$ $T_j=25\text{ }^{\circ}\text{C}$	180° half-sine wave; $t_p=8.3\text{ ms}$; single pulse; $V_D=V_R=0\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$
I^2t	Safety factor	$\text{A}^2\text{s}\cdot 10^3$	3300 4500	$T_j=T_{j\max}$ $T_j=25\text{ }^{\circ}\text{C}$	180° half-sine wave; $t_p=10\text{ ms}$; single pulse; $V_D=V_R=0\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$
			3000 3900	$T_j=T_{j\max}$ $T_j=25\text{ }^{\circ}\text{C}$	180° half-sine wave; $t_p=8.3\text{ ms}$; single pulse; $V_D=V_R=0\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3800...4400	$T_{j\min}<T_j<T_{j\max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3900...4500	$T_{j\min}<T_j<T_{j\max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6\cdot V_{DRM}$ $0.6\cdot V_{RRM}$	$T_j=T_{j\max}$; Gate open	

TRIGGERING					
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	5	$T_j=T_{j\max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	630	$T_j=T_{j\max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\ \mu$ s; $di_G/dt\geq 1\text{ A}/\mu$ s	
THERMAL					
T_{stg}	Storage temperature	$^{\circ}\text{C}$	-60...+50		
T_j	Operating junction temperature	$^{\circ}\text{C}$	-60...+125		
MECHANICAL					
F	Mounting force	kN	33.0...40.0		
a	Acceleration	m/s ²	50	Device clamped	

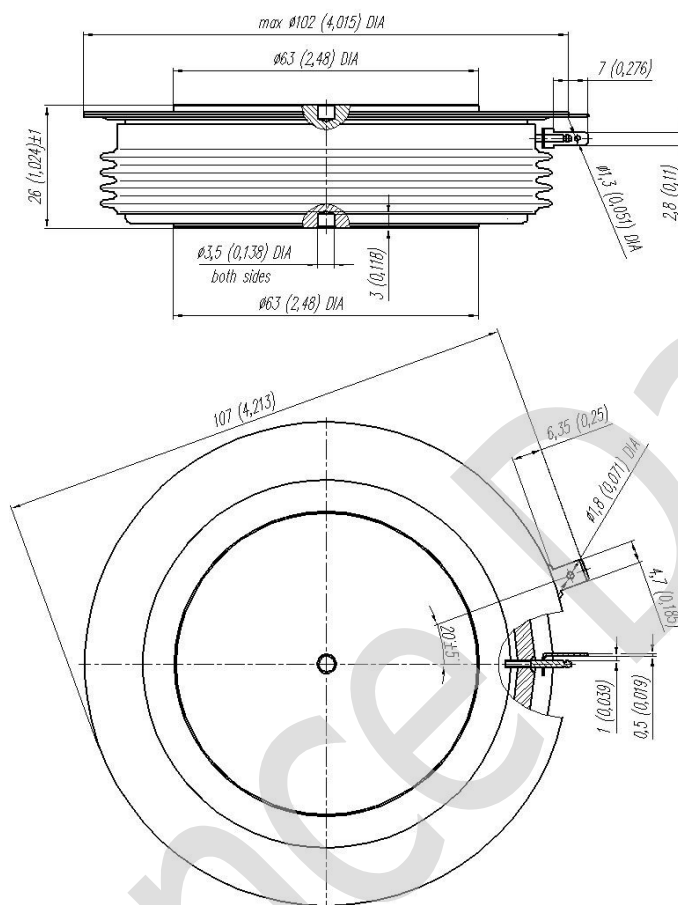
CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.30	$T_j=25\text{ }^{\circ}\text{C}$; $I_{TM}=5000\text{ A}$	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.05	$T_j=T_{j\text{ max}}$;	
r_T	On-state slope resistance, max	$\text{m}\Omega$	0.250	$0.5\pi I_{TAV} < I_T < 1.5\pi I_{TAV}$	
I_L	Latching current, max	mA	1500	$T_j=25\text{ }^{\circ}\text{C}$; $V_D=12\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$	
I_H	Holding current, max	mA	300	$T_j=25\text{ }^{\circ}\text{C}$; $V_D=12\text{ V}$; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	$T_j=T_{j\text{ max}}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	$\text{V}/\mu\text{s}$	1000	$T_j=T_{j\text{ max}}$; $V_D=0.67\cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	5.00 3.00 2.00	$T_j= T_{j\text{ min}}$ $T_j=25\text{ }^{\circ}\text{C}$ $T_j= T_{j\text{ max}}$	$V_D=12\text{ V}$; $I_D=3\text{ A}$; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 200	$T_j= T_{j\text{ min}}$ $T_j= 25\text{ }^{\circ}\text{C}$ $T_j= T_{j\text{ max}}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j=T_{j\text{ max}}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	15.00		
SWITCHING					
t_{gd}	Delay time	μs	4.00	$T_j=25\text{ }^{\circ}\text{C}$; $V_D=0.4\cdot V_{DRM}$; $I_{TM}=I_{TAV}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$	
t_q	Turn-off time ²⁾ , max	μs	630	$dv_D/dt=50\text{ V}/\mu\text{s}$; $T_j=T_{j\text{ max}}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10\text{ A}/\mu\text{s}$; $V_R=100\text{ V}$; $V_D=0.67\text{ }V_{DRM}$;	

THERMAL					
R _{thjc}	Thermal resistance, junction to case, max	°C/W	0.0100	Direct current	Double side cooled
R _{thjc-A}			0.0220		Anode side cooled
R _{thjc-K}			0.0180		Cathode side cooled
R _{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0030	Direct current	
MECHANICAL					
m	Weight, max	g	820		
D _s	Surface creepage distance	mm (inch)	36.50 (1.437)		
D _a	Air strike distance	mm (inch)	16.5 (0.650)		

PART NUMBERING GUIDE						
T	163	1250	44	A2	C2	N
1	2	3	4	5	6	7
1. Phase Control Thyristor						
2. Design version						
3. Mean on-state current, A						
4. Voltage code						
5. Critical rate of rise of off-state voltage, V/μs						
6. Turn-off time (dv _D /dt=50 V/μs)						
7. Ambient conditions: N – normal; T – tropical						

NOTES	
1) Critical rate of rise of off-state voltage	
Symbol of Group	A2
(dv _D /dt) _{crit} , V/μs	1000
2) Turn-off time (dv _D /dt=50 V/μs)	
Symbol of Group	C2
t _q , μs	630



All dimensions in millimeters (inches)