High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Chip
Type TG56-500-65

Maximum allowable mean on-state current[1)]					I_{TAV}		500 A				
Repetitive peak off-state voltage					V_{DRM}		4600...6500 V				
Repetitive peak reverse voltage					V_{RRM}						
Turn-off time					t_q		800 µs				
V_{DRM}, V_{RRM}, V	4600	4800	5000	5200	5400	5600	5800	6000	6200	6400	6500
Voltage code	46	48	50	52	54	56	58	60	62	64	65
T_j, °C	–60...+125										

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current[1)]	A	500 696	T_c=101 °C, Double side cooled T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current[1)]	A	785	T_c=101 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current[1)]	kA	9.5 11.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			10.0 11.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor[1)]	$A^2s{\cdot}10^3$	450 600	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			410 540	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	4600...6500	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	4700...6600	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.6·V_{DRM} 0.6·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	4	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	400	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; I_{TM}=2150 A; Gate pulse: I_G=2 A; t_{GP}=50 µs; $di_G/dt \geq 2$ A/µs
THERMAL				
T_{stg}	Storage temperature	°C	–60...+50	
T_j	Operating junction temperature	°C	–60...+125	
MECHANICAL				
F	Mounting force[1)]	kN	24.0...28.0	
F_{cg}	Force on control gate	N	7.8	

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage[1)], max	V	2.50	T_j=25 °C; I_{TM}=1570 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.272	$T_j=T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance[1)], max	mΩ	1.125		
I_L	Latching current, max	mA	1500	T_j=25 °C; V_D=12 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; $di_G/dt \geq 1$ A/µs	
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[2)], min	V/µs	1000, 1600, 2000, 2500	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	$T_j=T_{j\,min}$ T_j=25 °C $T_j=T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	400 250 150	$T_j=T_{j\,min}$ T_j= 25 °C $T_j=T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.45	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	65.00		
SWITCHING					
t_{gd}	Delay time, max	µs	3.00	T_j=25 °C; V_D=1500 V; $I_{TM}=I_{TAV}$; di/dt=200 A/µs; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs	
t_{gt}	Turn-on time, max	µs	10.00		
t_q	Turn-off time[3)], max	µs	800	dv_D/dt=50 V/µs; $T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; di_R/dt=-5 A/µs; V_R=100V; $V_D=0.67 \cdot V_{DRM}$	

THERMAL					
R_{thjc}	Thermal resistance, junction to case[1], max	°C/W	0.0180	Direct current	Double side cooled
R_{thjc-A}			0.0396		Anode side cooled
R_{thjc-K}			0.0324		Cathode side cooled
MECHANICAL					
m	Weight, max	g	75.80		

PART NUMBERING GUIDE

TG	56	500	65	A2	B2
1	2	3	4	5	6

1. Phase Control Thyristor Chip with a distributed gate
2. Maximum diameter, mm
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage, V/μs
6. Turn-off time (dv_D/dt=50 V/μs)

NOTES

[1] Depending on the specifications of the housing used. The specified values are relevant when using the Proton-Electrotex T.D5 housing.

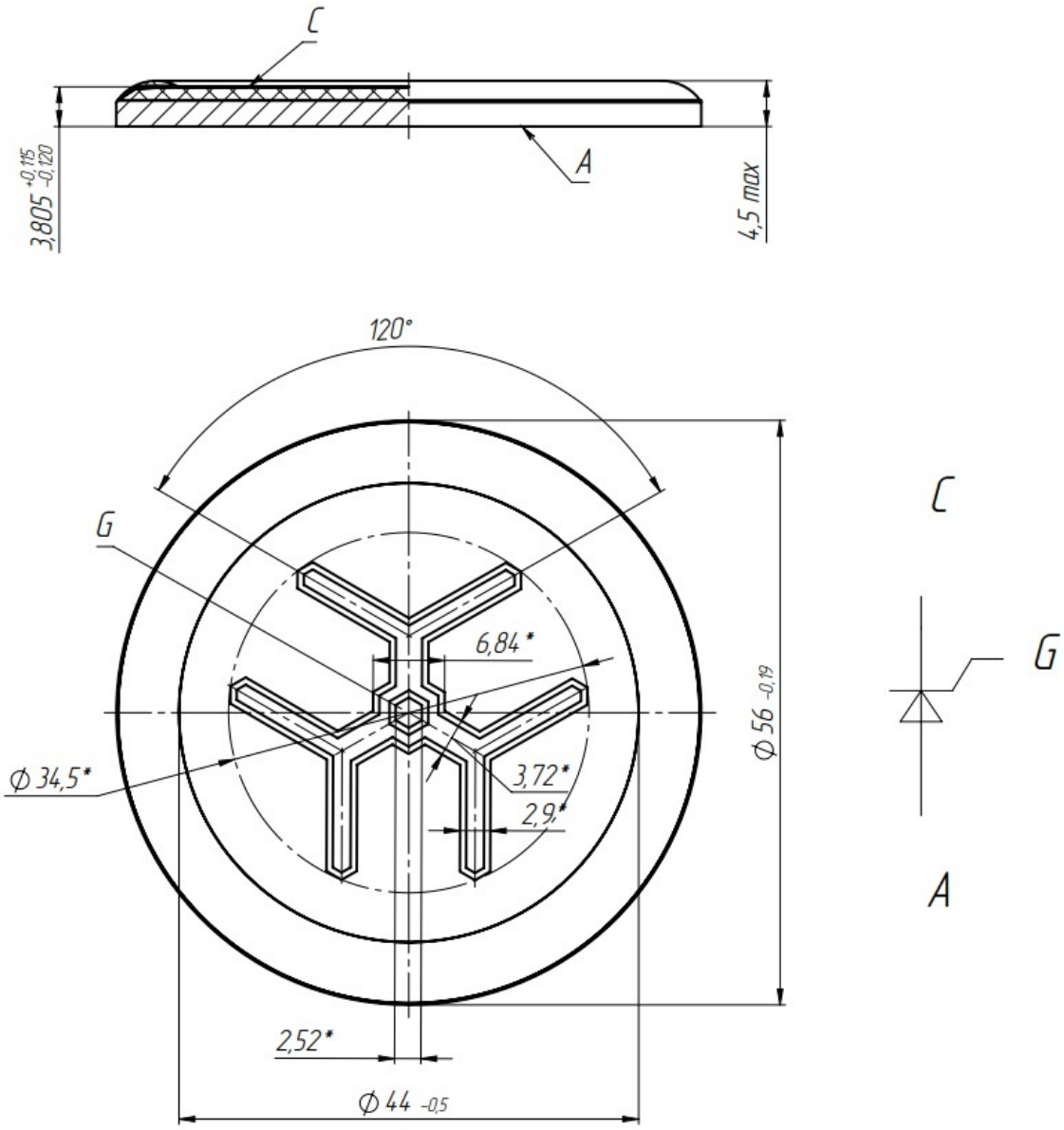
[2] Critical rate of rise of off-state voltage

Symbol of Group	A2	T1	P1	M1
$(dv_D/dt)_{crit}$, V/μs	1000	1600	2000	2500

[3] Turn-off time (dv_D/dt=50 V/μs)

Symbol of Group	B2
t_q, μs	800

OVERALL DIMENSIONS



All dimensions in millimeters

The information contained herein is confidential and protected by Copyright.
In the interest of product improvement, Proton-Electrotex reserves the right to change data sheet without notice.