



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Chip
Type TG70-1000-52

Maximum allowable mean on-state current ¹⁾		I _{TAV}		1000 A	
Repetitive peak off-state voltage		V _{DRM}		4600...5200 V	
Repetitive peak reverse voltage		V _{RRM}			
Turn-off time		t _q		800 μs	
V _{DRM} , V _{RRM} , V	4600	4800	5000	5200	
Voltage code	46	48	50	52	
T _j , °C	-60...+125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current ¹⁾	A	1000 1476	$T_c=104\text{ }^{\circ}\text{C}$, Double side cooled $T_c=85\text{ }^{\circ}\text{C}$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current ¹⁾	A	1570	$T_c=104\text{ }^{\circ}\text{C}$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current ¹⁾	kA	21.0 24.0	$T_j=T_{j\max}$ $T_j=25\text{ }^{\circ}\text{C}$	180° half-sine wave; $t_p=10\text{ ms}$; single pulse; $V_D=V_R=0\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$
			22.0 25.0	$T_j=T_{j\max}$ $T_j=25\text{ }^{\circ}\text{C}$	180° half-sine wave; $t_p=8.3\text{ ms}$; single pulse; $V_D=V_R=0\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$
I^2t	Safety factor ¹⁾	$\text{A}^2\text{s}\cdot 10^3$	2200 2800	$T_j=T_{j\max}$ $T_j=25\text{ }^{\circ}\text{C}$	180° half-sine wave; $t_p=10\text{ ms}$; single pulse; $V_D=V_R=0\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$
			2000 2500	$T_j=T_{j\max}$ $T_j=25\text{ }^{\circ}\text{C}$	180° half-sine wave; $t_p=8.3\text{ ms}$; single pulse; $V_D=V_R=0\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	4600...5200	$T_{j\min}<T_j<T_{j\max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	4700...5300	$T_{j\min}<T_j<T_{j\max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6\cdot V_{DRM}$ $0.6\cdot V_{RRM}$	$T_j=T_{j\max}$; Gate open	

TRIGGERING					
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	5	$T_j=T_{j\max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	630	$T_j=T_{j\max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2 I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50\ \mu$ s; $di_G/dt\geq 2$ A/ μ s	
THERMAL					
T_{stg}	Storage temperature	$^{\circ}$ C	-60...+50		
T_j	Operating junction temperature	$^{\circ}$ C	-60...+125		
MECHANICAL					
F	Mounting force ¹⁾	kN	33.0...40.0		
F_{cg}	Force on control gate	N	7.8		

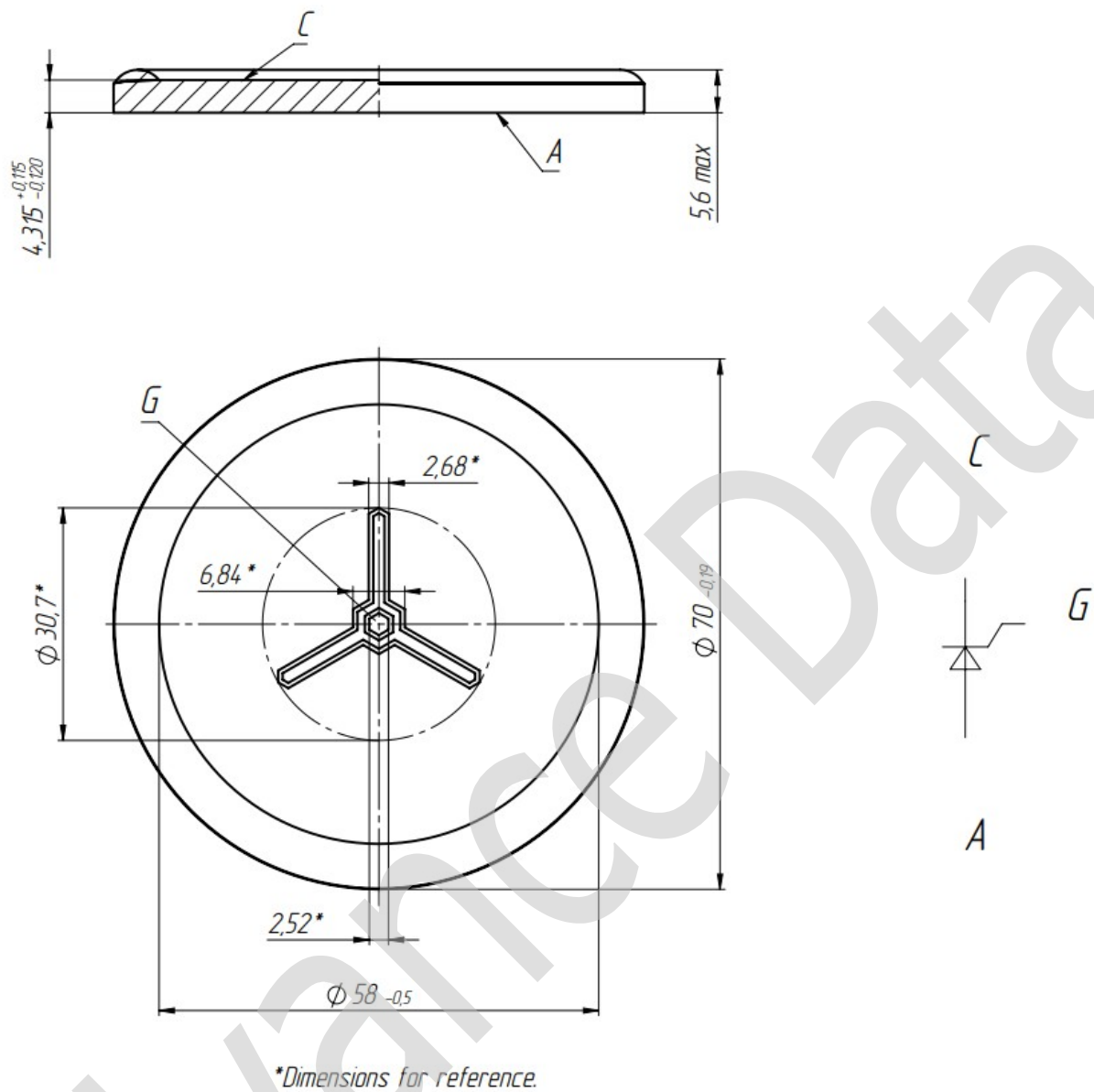
CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage ¹⁾ , max	V	2.80	$T_j=25\text{ }^{\circ}\text{C}$; $I_{TM}=5000\text{ A}$	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.900	$T_j=T_{j\text{ max}}$;	
r_T	On-state slope resistance ¹⁾ , max	m Ω	0.500	$0.5\pi I_{TAV} < I_T < 1.5\pi I_{TAV}$	
I_L	Latching current, max	mA	1500	$T_j=25\text{ }^{\circ}\text{C}$; $V_D=12\text{ V}$; Gate pulse: $I_G=2\text{ A}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt\geq 1\text{ A}/\mu\text{s}$	
I_H	Holding current, max	mA	300	$T_j=25\text{ }^{\circ}\text{C}$; $V_D=12\text{ V}$; Gate open	
BLOCKING					
I_{DRM} , I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	$T_j=T_{j\text{ max}}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ²⁾ , min	V/ μs	1000	$T_j=T_{j\text{ max}}$; $V_D=0.67\cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	5.00 3.00 2.00	$T_j= T_{j\text{ min}}$ $T_j=25\text{ }^{\circ}\text{C}$ $T_j= T_{j\text{ max}}$	$V_D=12\text{ V}$; $I_D=3\text{ A}$; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 200	$T_j= T_{j\text{ min}}$ $T_j= 25\text{ }^{\circ}\text{C}$ $T_j= T_{j\text{ max}}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j=T_{j\text{ max}}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	15.00		
SWITCHING					
t_{gd}	Delay time, max	μs	4.00	$T_j=25\text{ }^{\circ}\text{C}$; $V_D=1500\text{ V}$; $I_{TM}=I_{TAV}$; $di/dt=200\text{ A}/\mu\text{s}$; Gate pulse: $I_G=2\text{ A}$; $V_G=20\text{ V}$; $t_{GP}=50\text{ }\mu\text{s}$; $di_G/dt=2\text{ A}/\mu\text{s}$	
t_q	Turn-off time ³⁾ , max	μs	800	$dv_D/dt=50\text{ V}/\mu\text{s}$; $T_j=T_{j\text{ max}}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10\text{ A}/\mu\text{s}$; $V_R=100\text{ V}$; $V_D=0.67\text{ }V_{DRM}$;	

THERMAL					
R _{thjc}	Thermal resistance, junction to case ¹⁾ , max	°C/W	0.0100	Direct current	Double side cooled
R _{thjc-A}			0.0220		Anode side cooled
R _{thjc-K}			0.0180		Cathode side cooled
MECHANICAL					
m	Weight, max	g	193		

PART NUMBERING GUIDE						NOTES
TG	70	1000	52	A2	B2	¹⁾ Depending on the specifications of the housing used. The specified values are relevant when using the Proton-Electrotex T.E3 housing. ²⁾ Critical rate of rise of off-state voltage
1	2	3	4	5	6	
1. Phase Control Thyristor Chip with a distributed gate 2. Maximum diameter, mm 3. Mean on-state current, A 4. Voltage code 5. Critical rate of rise of off-state voltage, V/μs 6. Turn-off time (dv_D/dt=50 V/μs)						
						Symbol of group (dv_D/dt)_{crit}, V/μs A2 1000
						Symbol of group t_q, μs B2 800

OVERALL DIMENSIONS



All dimensions in millimeters