



PROTON-ELECTROTEX RUSSIA

High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Chip Type TR40-800-18

Maximum allowable mean on-state current ¹⁾				I_{TAV}	800 A			
Repetitive peak off-state voltage				V_{DRM}	1000...1800 V			
Repetitive peak reverse voltage				V_{RRM}				
Turn-off time				t_q	160, 200, 250, 320, 400, 500 μ s			
V_{DRM}, V_{RRM}, V	1000	1100	1200	1300	1400	1500	1600	1800
Voltage code	10	11	12	13	14	15	16	18
$T_j, ^\circ\text{C}$	-60...+125							

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I _{TAV}	Maximum allowable mean on-state current ¹⁾	A	800 796	T _c =84 °C, Double side cooled T _c =85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I _{TRMS}	RMS on-state current ¹⁾	A	1256	T _c =84 °C, Double side cooled 180° half-sine wave; 50 Hz	
I _{TSM}	Surge on-state current ¹⁾	kA	14.0 16.0	T _j =T _{j max} T _j =25 °C	180° half-sine wave; t _p =10 ms; single pulse; V _D =V _R =0 V; Gate pulse: I _G =2 A; t _{GP} =50 μs; di _G /dt≥1 A/μs
			15.0 17.0	T _j =T _{j max} T _j =25 °C	180° half-sine wave; t _p =8.3 ms; single pulse; V _D =V _R =0 V; Gate pulse: I _G =2 A; t _{GP} =50 μs; di _G /dt≥1 A/μs
I ² t	Safety factor ¹⁾	A ² s·10 ³	980 1280	T _j =T _{j max} T _j =25 °C	180° half-sine wave; t _p =10 ms; single pulse; V _D =V _R =0 V; Gate pulse: I _G =2 A; t _{GP} =50 μs; di _G /dt≥1 A/μs
			930 1190	T _j =T _{j max} T _j =25 °C	180° half-sine wave; t _p =8.3 ms; single pulse; V _D =V _R =0 V; Gate pulse: I _G =2 A; t _{GP} =50 μs; di _G /dt≥1 A/μs
BLOCKING					
V _{DRM} , V _{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	1000...1800	T _{j min} < T _j < T _{j max} ; 180° half-sine wave; 50 Hz; Gate open	
V _{DSM} , V _{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	1100...1900	T _{j min} < T _j < T _{j max} ; 180° half-sine wave; single pulse; Gate open	
V _D , V _R	Direct off-state and Direct reverse voltages	V	0.6·V _{DRM} 0.6·V _{RRM}	T _j =T _{j max} ; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j = T_{j\max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	4	$T_j = T_{j\max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive ($f=1\text{ Hz}$)	A/ μs	1250	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 2000\text{ A}$; Gate pulse: $I_G = 2\text{ A}$; $t_{GP} = 50\text{ }\mu\text{s}$; $di_G/dt \geq 2\text{ A}/\mu\text{s}$
THERMAL				
T_{stg}	Storage temperature	$^{\circ}\text{C}$	$-60 \dots +50$	
T_j	Operating junction temperature	$^{\circ}\text{C}$	$-60 \dots +125$	
MECHANICAL				
F	Mounting force ¹⁾	kN	14.0...16.0	
F_{cg}	Force on control gate	N	7.8	

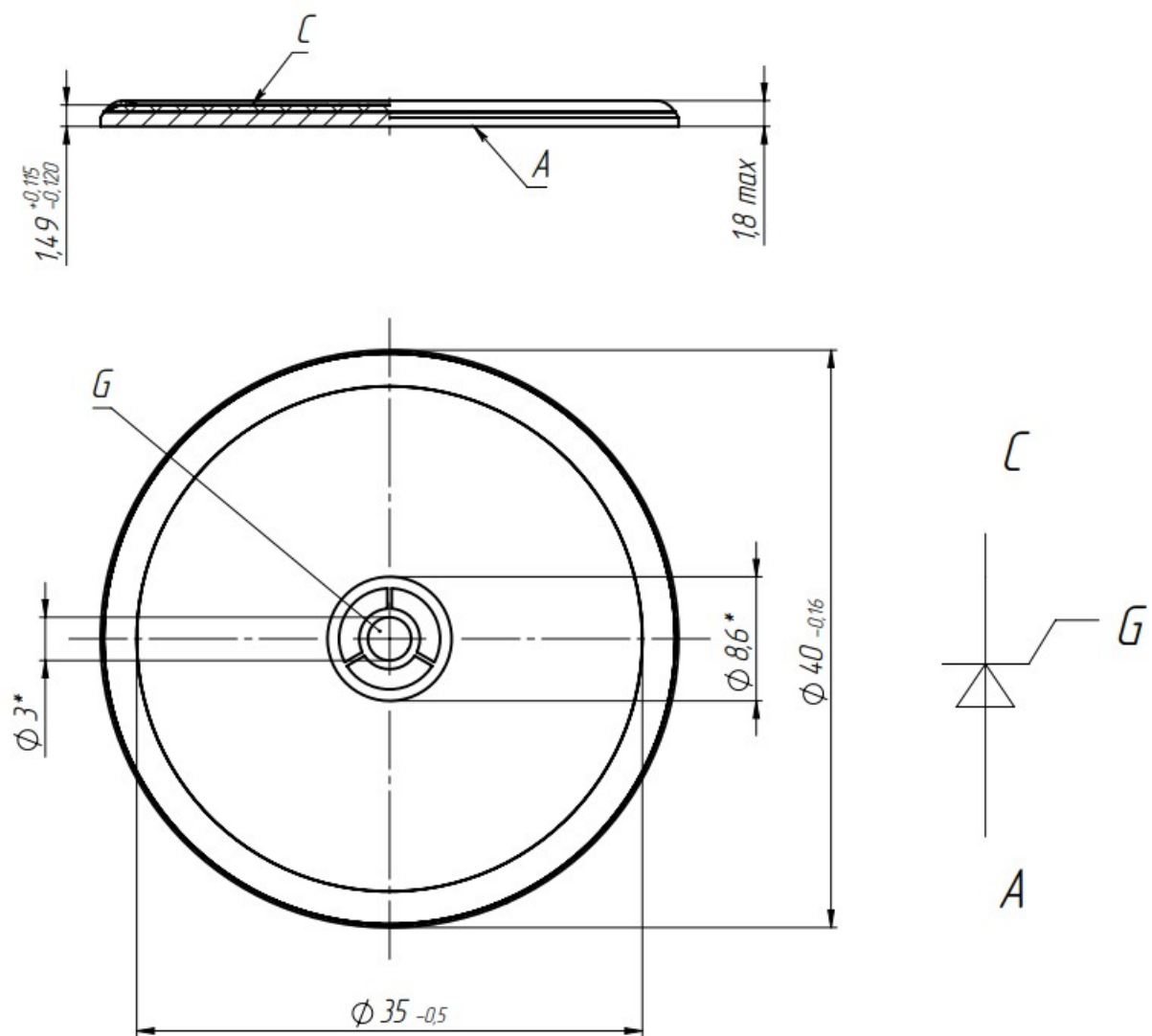
CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V _{TM}	Peak on-state voltage ¹⁾ , max	V	1.70	T _j =25 °C; I _{TM} =2512 A	
V _{T(TO)}	On-state threshold voltage, max	V	0.938	T _j =T _{j max} ;	
r _T	On-state slope resistance ¹⁾ , max	mΩ	0.323	0.5 π I _{TAV} < I _T < 1.5 π I _{TAV}	
I _L	Latching current, max	mA	1000	T _j =25 °C; V _D =12 V; Gate pulse: I _G =2 A; t _{GP} =50 μs; di _G /dt≥1 A/μs	
I _H	Holding current, max	mA	300	T _j =25 °C; V _D =12 V; Gate open	
BLOCKING					
I _{DRM} , I _{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	100	T _j =T _{j max} ; V _D =V _{DRM} ; V _R =V _{RRM}	
(dv _D /dt) _{crit}	Critical rate of rise of off-state voltage ²⁾ , min	V/μs	200, 320, 500, 1000, 1600, 2000, 2500	T _j =T _{j max} ; V _D =0.67·V _{DRM} ; Gate open	
TRIGGERING					
V _{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	T _j = T _{j min} T _j =25 °C T _j = T _{j max}	V _D =12 V; I _D =3 A; Direct gate current
I _{GT}	Gate trigger direct current, max	mA	400 250 150	T _j = T _{j min} T _j = 25 °C T _j = T _{j max}	
V _{GD}	Gate non-trigger direct voltage, min	V	0.30	T _j =T _{j max} ; V _D =0.67·V _{DRM} ;	
I _{GD}	Gate non-trigger direct current, min	mA	35.00	Direct gate current	
SWITCHING					
t _{gd}	Delay time, max	μs	0.80	T _j =25 °C; V _D =1000 V; I _{TM} =I _{TAV} ; di/dt=200 A/μs;	
t _{gt}	Turn-on time, max	μs	3.00	Gate pulse: I _G =2 A; V _G =20 V; t _{GP} =50 μs; di _G /dt=2 A/μs	
t _q	Turn-off time ³⁾ , max	μs	160, 200, 250, 320, 400, 500	dv _D /dt=50 V/μs; T _j =T _{j max} ; I _{TM} = I _{TAV} ; di _R /dt=-10 A/μs; V _R =100V; V _D =0.67·V _{DRM}	

THERMAL					
R _{thjc}	Thermal resistance, junction to case ¹⁾ , max	°C/W	0.0320	Direct current	Double side cooled
R _{thjc-A}			0.0704		Anode side cooled
R _{thjc-K}			0.0576		Cathode side cooled
MECHANICAL					
m	Weight, max	g	15.30		

PART NUMBERING GUIDE						NOTES																															
TR	40	800	18	A2	E2	1) Depending on the specifications of the housing used. The specified values are relevant when using the Proton-Electrotex T.C2 housing. 2) Critical rate of rise of off-state voltage <table><tr><th>Symbol of Group</th><th>P2</th><th>K2</th><th>E2</th><th>A2</th><th>T1</th><th>P1</th><th>M1</th></tr><tr><td>$(dv_D/dt)_{crit}$, V/μs</td><td>200</td><td>320</td><td>500</td><td>1000</td><td>1600</td><td>2000</td><td>2500</td></tr></table> 3) Turn-off time ($dv_D/dt=50$ V/μs) <table><tr><th>Symbol of Group</th><th>T2</th><th>P2</th><th>M2</th><th>K2</th><th>H2</th><th>E2</th></tr><tr><td>t_{qr}, μs</td><td>160</td><td>200</td><td>250</td><td>320</td><td>400</td><td>500</td></tr></table>		Symbol of Group	P2	K2	E2	A2	T1	P1	M1	$(dv_D/dt)_{crit}$, V/μs	200	320	500	1000	1600	2000	2500	Symbol of Group	T2	P2	M2	K2	H2	E2	t_{qr} , μs	160	200	250	320	400	500
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1. Phase Control Thyristor Chip																																					
2. Maximum diameter, mm																																					
3. Mean on-state current, A																																					
4. Voltage code																																					
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OVERALL DIMENSIONS



**Dimensions for reference.*

All dimensions in millimeters

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