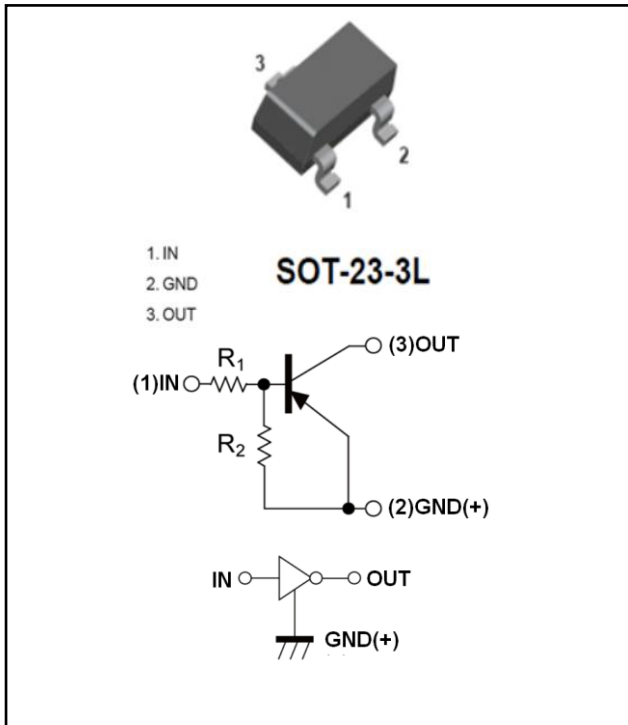


PNP Digital Transistors (Built-in Resistors)



Features

- Epoxy meets UL-94 V-0 flammability rating
- Moisture Sensitivity Level 1
- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors
- Surface mount package ideally Suited for Automatic Insertion

Mechanical Data

- **Package:** SOT-23-3L
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Marking:** E11

■Maximum Ratings (Ta=25°C Unless otherwise specified)

ITEM	SYMBOL	UNIT	VALUE
Supply Voltage	V_{CC}	V	-50
Input Voltage	V_{IN}	V	-10 to +5
Output Current	I_O	mA	-100
Power Dissipation	P_D	mW	200
Junction Temperature	T_J	°C	-55 to +150
Storage Temperature	T_{STG}	°C	-55 to +150



DTA113ZKA

■ Electrical Characteristics (Ta=25°C unless otherwise specified)

ITEM	SYMBOL	UNIT	CONDITIONS	MIN	TYP	MAX
Input voltage	$V_{I(off)}$	V	$V_{CC}=-5V, I_O=-100\mu A$	-0.3		
	$V_{I(on)}$	V	$V_O=-0.3V, I_O=-10mA$			-3
Output voltage	$V_{O(on)}$	V	$I_O/I_I=-10mA/-0.5mA$			-0.3
Output current	$I_{O(off)}$	μA	$V_{CC}=-50V, V_I=0$			-0.5
DC current gain	GI		$V_O=-5V, I_O=-5mA$	33		
Input resistance	R_1	k Ω		0.7	1.0	1.3
Resistance ratio	R_2/R_1			8	10	12
Transition frequency	fT	MHz	$V_{CE}=-10V, I_E=-5mA, f=100MHz$		250	

■ Thermal Characteristics

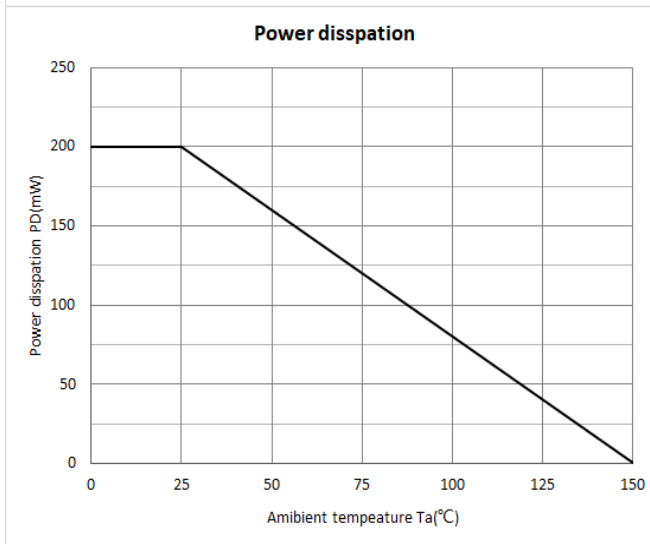
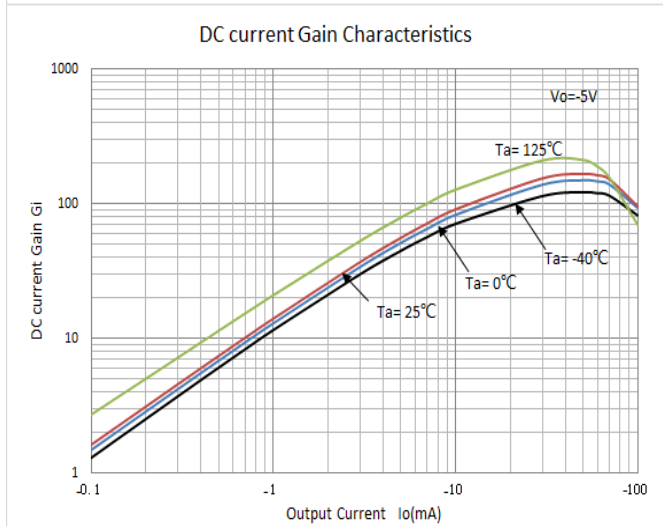
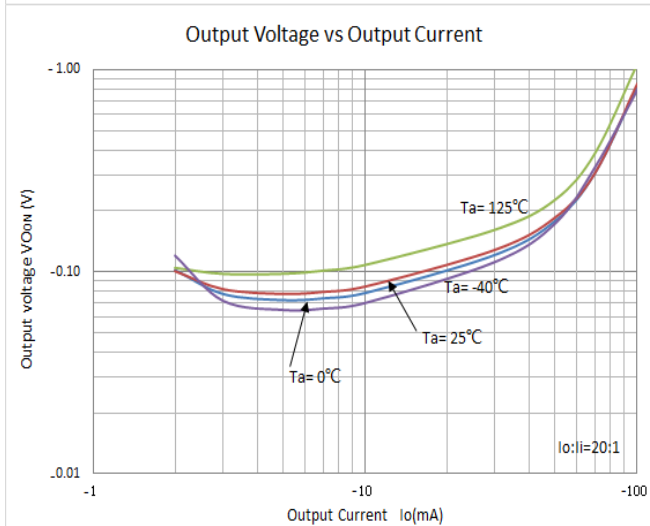
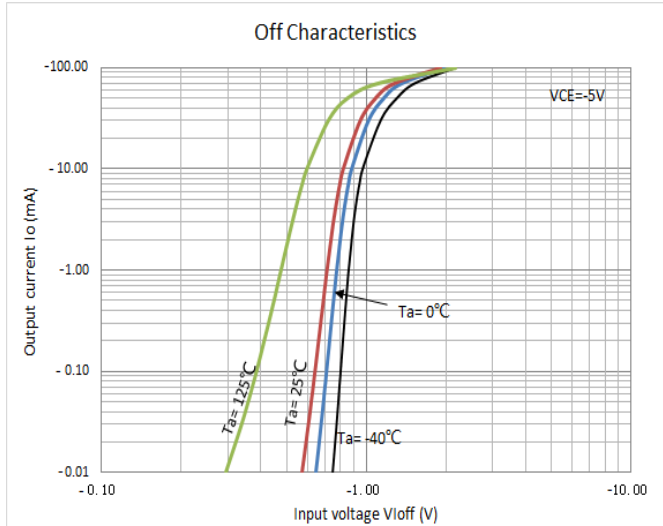
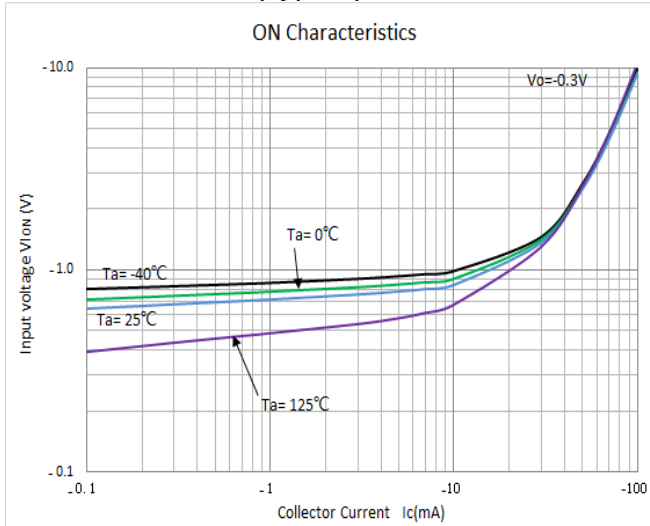
Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	$R_{\theta J-A}^{(1)}$	°C/W	625
Thermal resistance, junction-to-case	$R_{\theta J-C}^{(1)}$	°C/W	500

Note: (1) Device mounted on PCB, single-sided copper, with standard footprint.

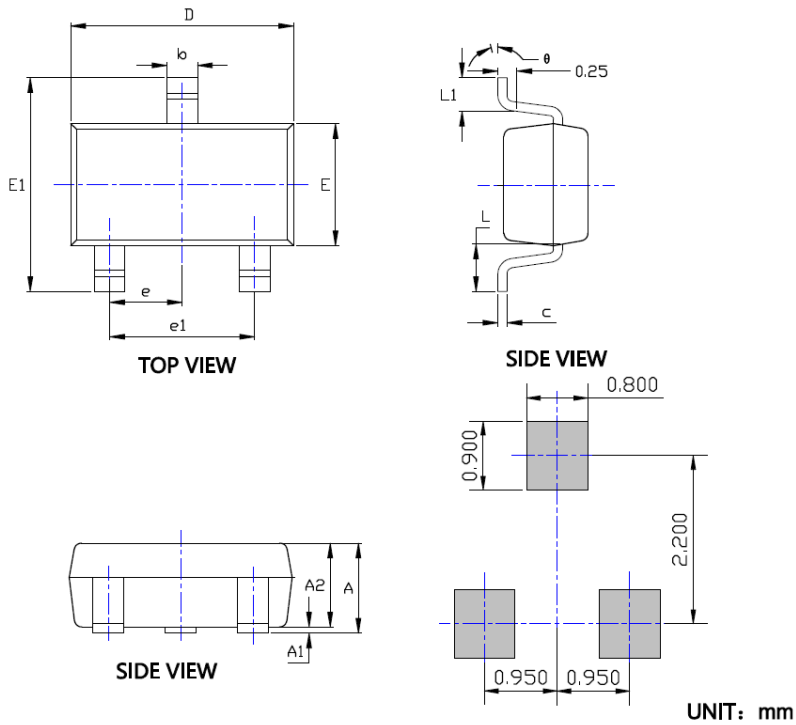
■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	UNIT WEIGHT(g)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
DTA113ZKA	F2	Approximate 0.014	3000	30000	120000	7" reel

■ Characteristics (Typical)



■SOT-23-3L Package Outline Dimensions



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.041	0.049	1.050	1.250
A1	0.000	0.008	0.000	0.200
A2	0.041	0.045	1.050	1.150
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.111	0.119	2.820	3.020
E	0.059	0.067	1.500	1.700
E1	0.104	0.116	2.650	2.950
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.024REF		0.600REF	
L1	0.012	0.024	0.300	0.600
∅	0°	8°	0°	8°

NOTE:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

SUGGESTED SOLDER PAD LAYOUT

Note:

- All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位，除非另有说明]
- General tolerances: $\pm 0.10\text{mm}$ unless otherwise specified.
[通用公差为 $\pm 0.10\text{mm}$ ，除非另有说明]
- Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
- All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
- Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
- Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸]
- Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面，共面性最大为0.1mm]
- ★It is the key size.
[★ 标记为关键尺寸]



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