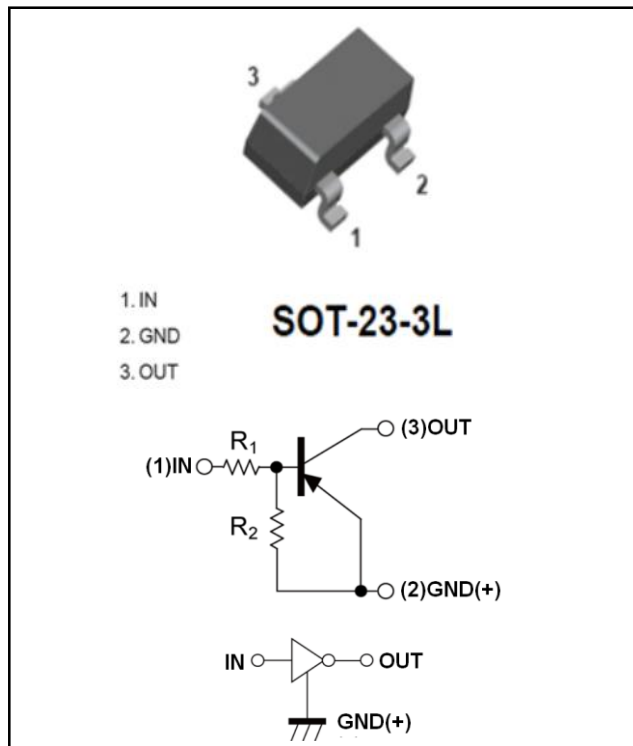


PNP Digital Transistors (Built-in Resistors)



Features

- Moisture sensitivity level 1
- Halogen free and RoHS compliant
- Surface mount package ideally suited for automatic insertion

Application

- Signal amplification
- Switching circuit

Mechanical data

- **Package**: SOT-23-3L
- **Terminals**: Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Marking**: AB

■ Maximum Ratings ($T_a=25^{\circ}\text{C}$ Unless otherwise specified)

Item	Symbol	Unit	Value
Supply voltage	V_{CC}	V	-50
Input voltage	V_{IN}	V	-40 to +10
Output current	I_O	mA	-100
Power dissipation	P_D	mW	200
Junction temperature	T_J	$^{\circ}\text{C}$	-55 to +150
Storage temperature	T_{STG}	$^{\circ}\text{C}$	-55 to +150



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■ Electrical Characteristics (T_a=25°C Unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Input voltage	V _{I(off)}	V	V _{CC} =-5V, I _O =-100uA	-0.5		
	V _{I(on)}	V	V _O =-0.3V, I _O =-1mA			-3.0
Output voltage	V _{O(on)}	V	I _O /I _I =-5mA/-0.25mA			-0.3
Input current	I _I	mA	V _I =-5V			-0.15
Output current	I _{O(off)}	uA	V _{CC} =-50V, V _I =0			-0.5
DC current gain	G _I		V _O =-5V, I _O =-5mA	80		
Input resistance	R ₁	kΩ		70	100	130
Resistance ratio	R ₂ /R ₁			0.8	1.0	1.2
Transition frequency	f _T	MHz	V _{CE} =-10V, I _E =-5mA, f=100MHz		250	

■ Thermal Characteristics

Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	R _{θJ-A} ⁽¹⁾	°C/W	625
Thermal resistance, junction-to-case	R _{θJ-C} ⁽¹⁾	°C/W	500

Note:

(1) Device mounted on PCB, single-sided copper, with standard footprint

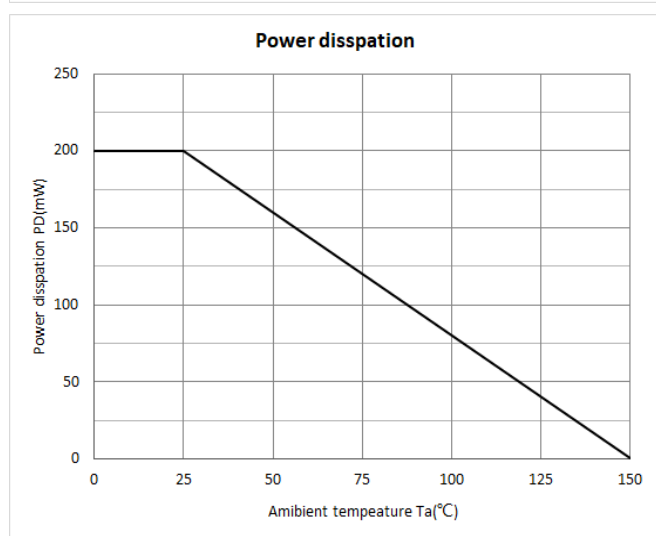
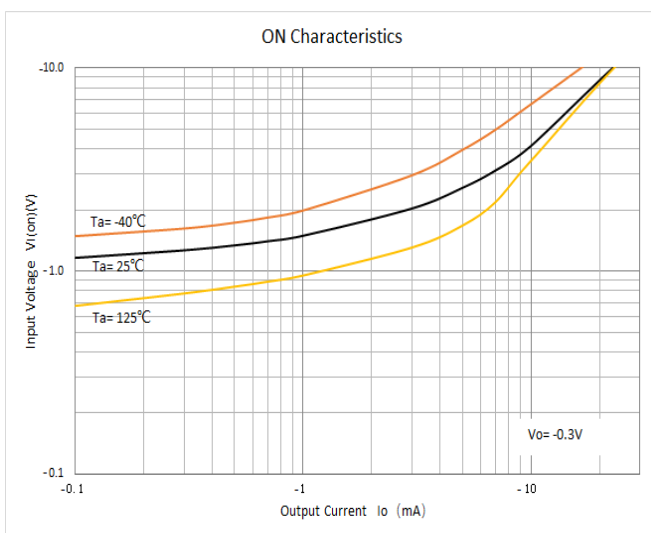
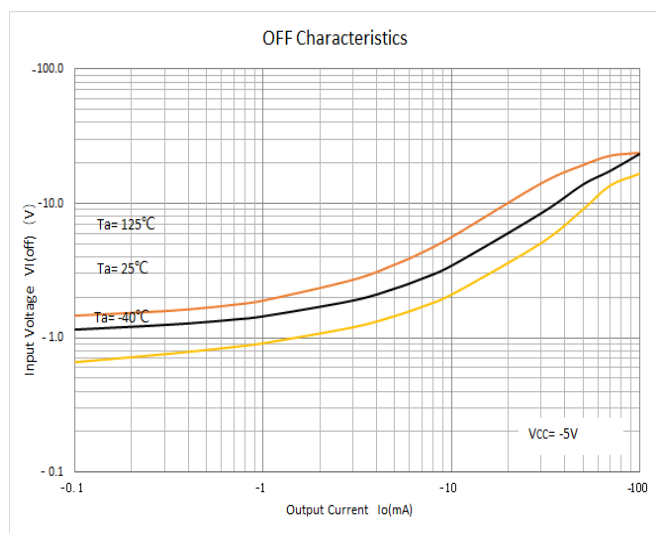
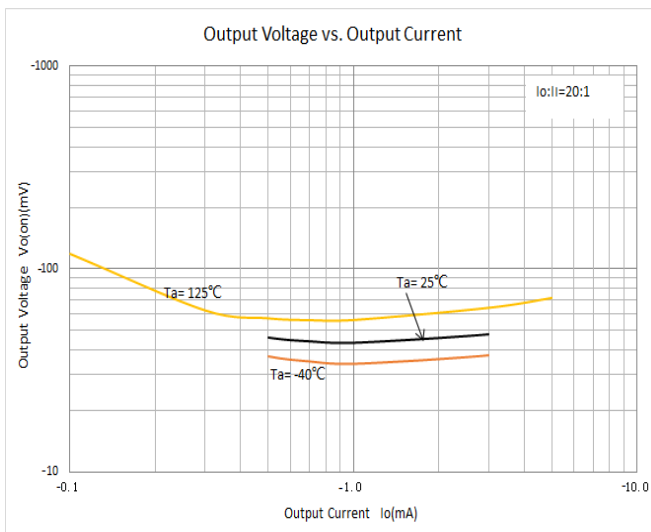
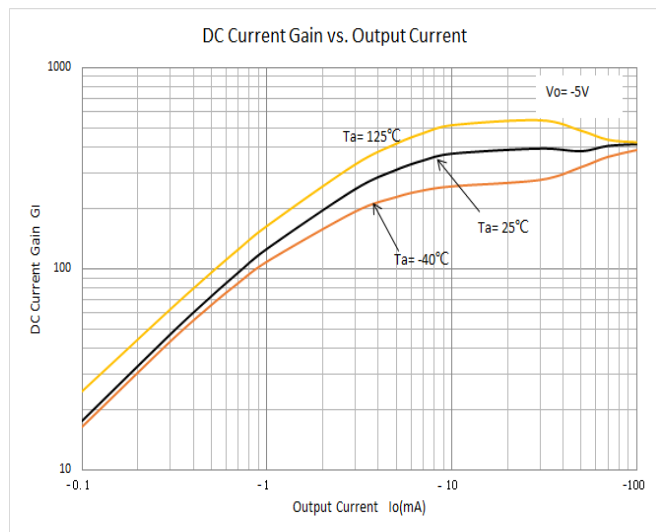
■ Ordering Information

Preferred P/N	Packing code	Unit weight(g)	Minimum package(pcs)	Inner box quantity(pcs)	Outer carton quantity(pcs)	Delivery mode
DTA115EKA	F2	Approximate 0.014	3000	30000	120000	7" reel



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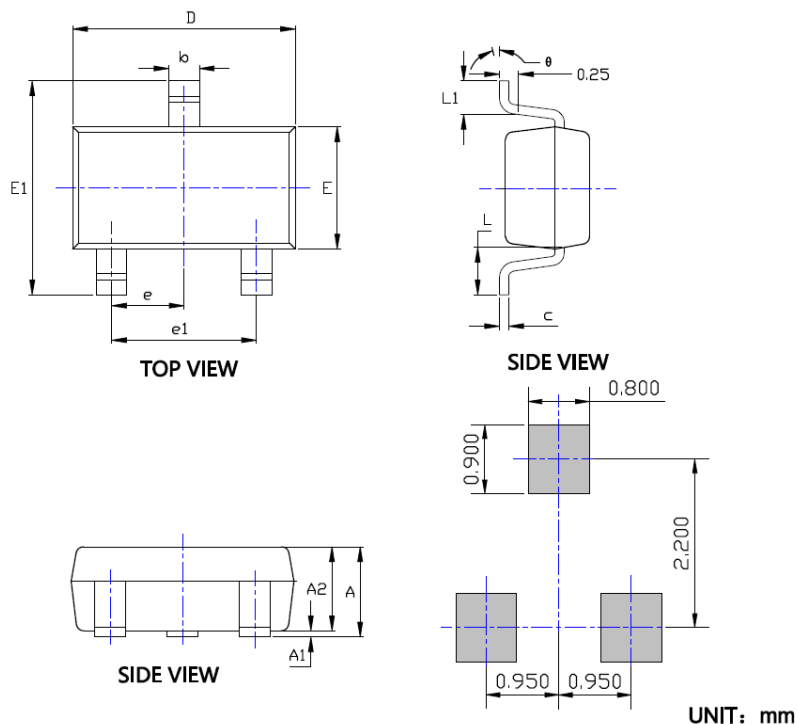
■ Characteristics (Typical)





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■ SOT-23-3L Package Outline Dimensions



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.041	0.049	1.050	1.250
A1	0.000	0.008	0.000	0.200
A2	0.041	0.045	1.050	1.150
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.111	0.119	2.820	3.020
E	0.059	0.067	1.500	1.700
E1	0.104	0.116	2.650	2.950
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.024REF		0.600REF	
L1	0.012	0.024	0.300	0.600
∅	0°	8°	0°	8°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位, 除非另有说明]
2. General tolerances: $\pm 0.10\text{mm}$ unless otherwise specified.
[通用公差为 $\pm 0.10\text{mm}$, 除非另有说明]
3. Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
4. All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
5. Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
6. Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[D和E是塑封体的外部极限尺寸, 不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺, 但是包含了包封错位的最大尺寸]
7. Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面, 共面性最大为0.1mm]
8. ★It is the key size.
[★ 标记为关键尺寸]



DTA115EKA

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