



P-Channel Enhancement Mode Field Effect Transistor

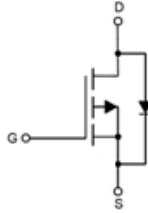


Top View



Bottom View

DFN1006-3L



Product Summary

• V_{DS}	-60V
• I_D	-0.22A
• $R_{DS(ON)}$ (at $V_{GS}=-10V$)	$<5\Omega$
• $R_{DS(ON)}$ (at $V_{GS}=-5V$)	$<6\Omega$
• ESD Level(HBM)	H0

General Description

- Low $R_{DS(ON)}$
- Low gate charge
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Video monitor
- Power management

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	-60	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} =-10V	I _D	-	-0.22	A
		T _A =100°C,V _{GS} =-10V		-	-0.14	
Pulsed Drain Current	T _A =25°C,t _p ≤10μs		I _{DM}	-	-0.88	
Maximum Body-Diode Continuous Current	T _A =25°C		I _S		-0.22	
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	0.47	W
		T _A =100°C		-	0.18	
Junction and Storage Temperature Range			T _J , T _{STG}	-55	150	°C

■ Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	265	$^{\circ}\text{C/W}$



YJA5K0P06A

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA, T _j =25°C	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V, T _j =25°C	-	-	-1	μA
		V _{DS} =-60V, V _{GS} =0V, T _j =125°C	-	-	-100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _j =25°C	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA, T _j =25°C	-0.9	-1.4	-2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-0.1A, T _j =25°C	-	2.8	5	Ω
		V _{GS} =-5V, I _D =-0.1A, T _j =25°C	-	3.2	6	Ω
Diode Forward Voltage	V _{SD}	I _S =-0.115A, V _{GS} =0V, T _j =25°C	-	-0.84	-1.2	V
Gate Resistance	R _G	f=1MHz, T _j =25°C	-	40	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, f=1MHz, T _j =25°C	-	22.9	-	pF
Output Capacitance	C _{oss}		-	2.9	-	
Reverse Transfer Capacitance	C _{rss}		-	1.56	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-30V, I _D =-0.19A, T _j =25°C	-	2.7	-	nC
Gate-Source Charge	Q _{gs}		-	0.6	-	
Gate-Drain Charge	Q _{gd}		-	0.9	-	
Reverse Recovery Charge	Q _{rr}	I _F =-0.19A, di/dt=100A/μs, V _{GS} =0V, V _R =-30V, T _j =25°C	-	4.4	-	nC
Reverse Recovery Time	t _{rr}		-	12	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DS} =-30V, I _D =-0.19A, R _{GEN} =3Ω, T _j =25°C	-	4.3	-	ns
Turn-on Rise Time	t _r		-	5.8	-	
Turn-off Delay Time	t _{D(off)}		-	7	-	
Turn-off Fall Time	t _f		-	46.1	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.



■ Typical Electrical and Thermal Characteristics Diagrams

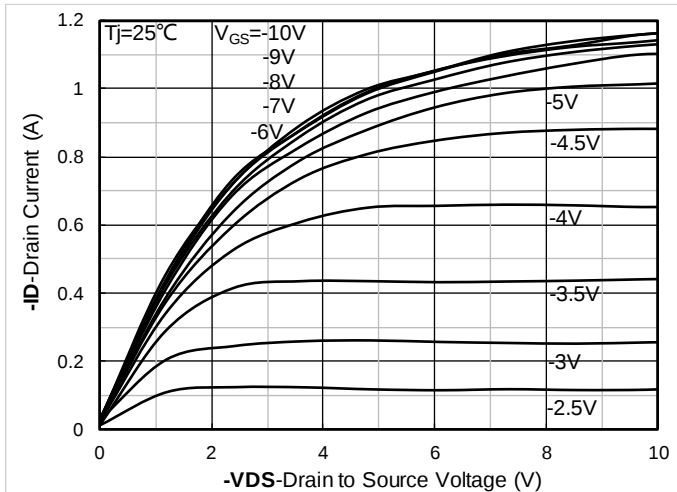


Figure 1. Output Characteristics; typical values

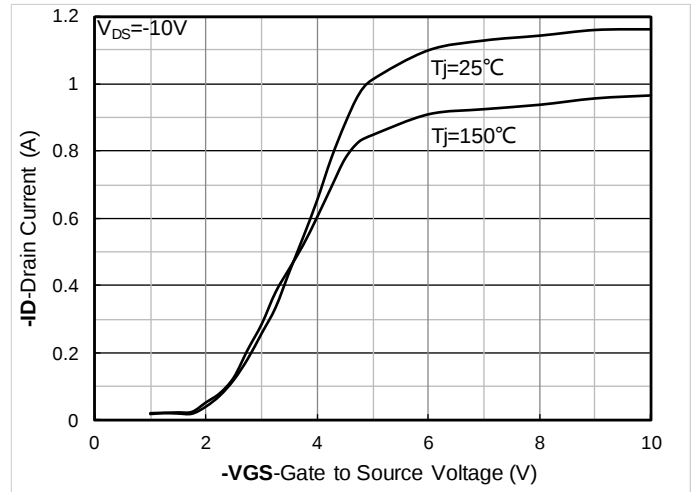


Figure 2. Transfer Characteristics; typical values

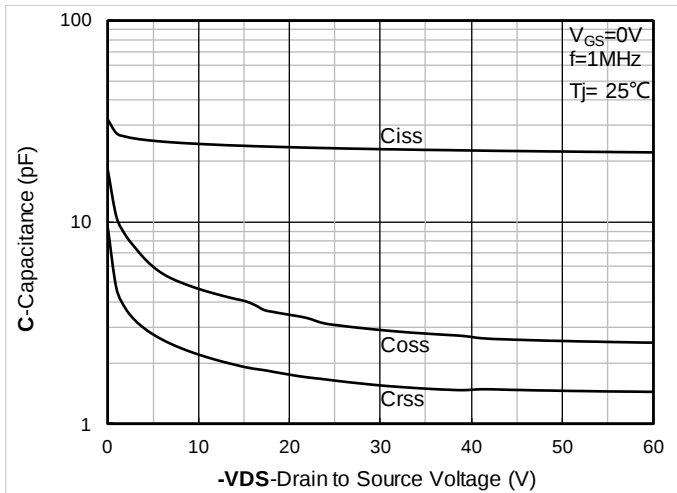


Figure 3. Capacitance Characteristics; typical values

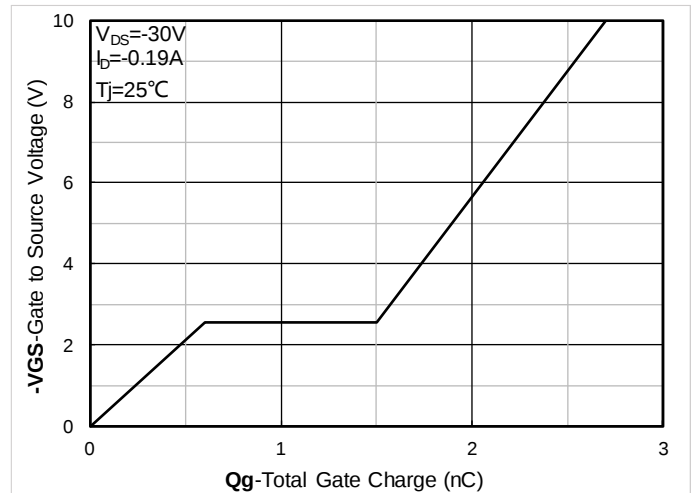


Figure 4. Gate Charge; typical values

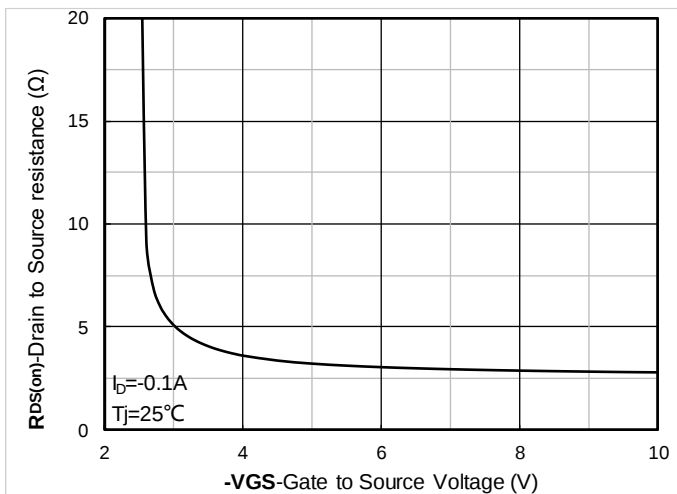


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

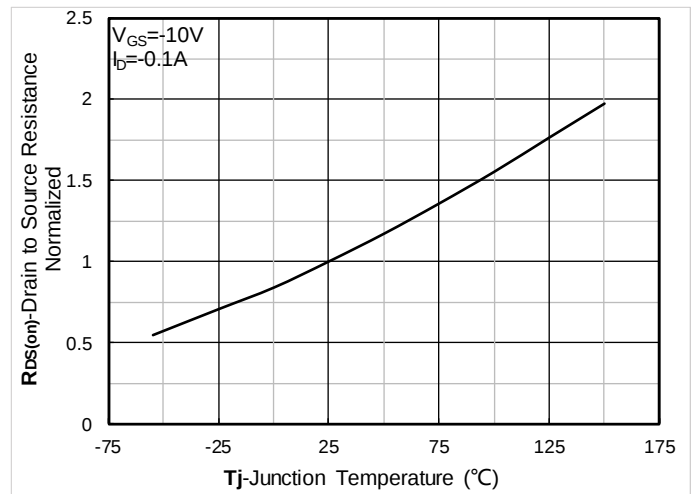


Figure 6. Normalized On-Resistance

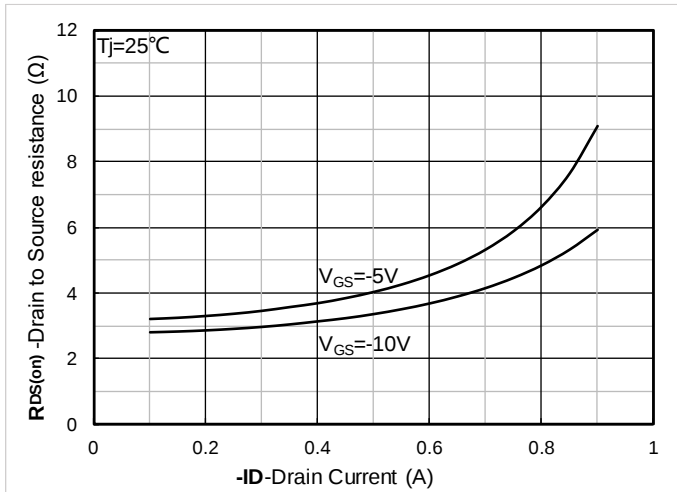


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

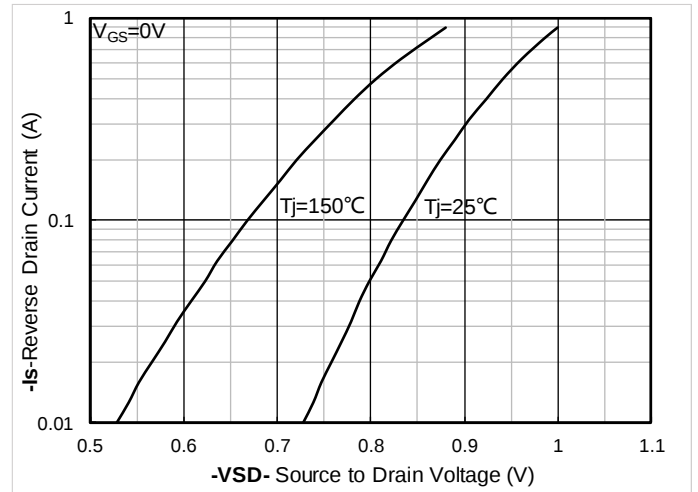


Figure 8. Forward characteristics of reverse diode; typical values

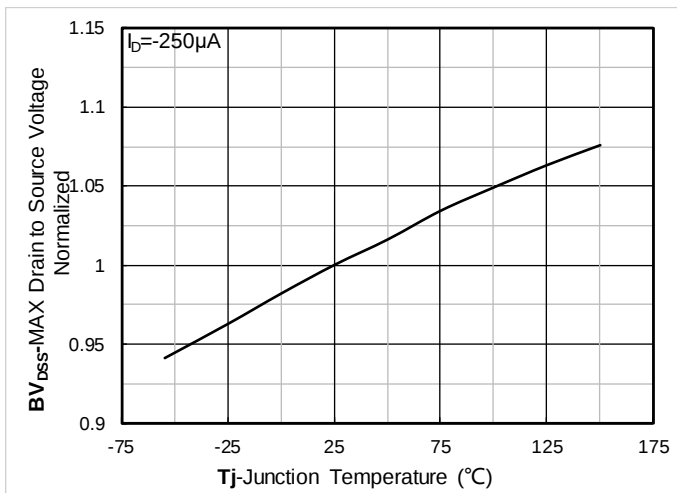


Figure 9. Normalized breakdown voltage

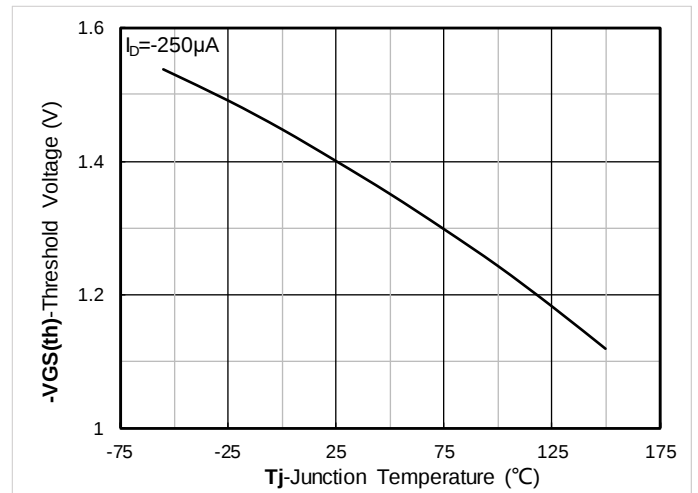


Figure 10. Gate Threshold voltage; typical values

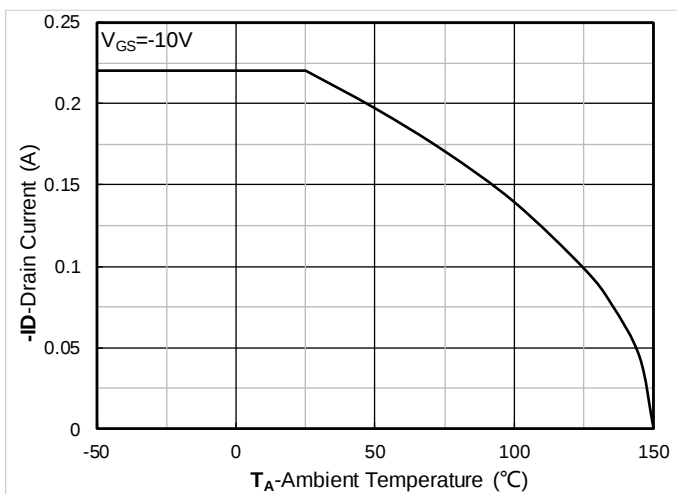


Figure 11. Current dissipation

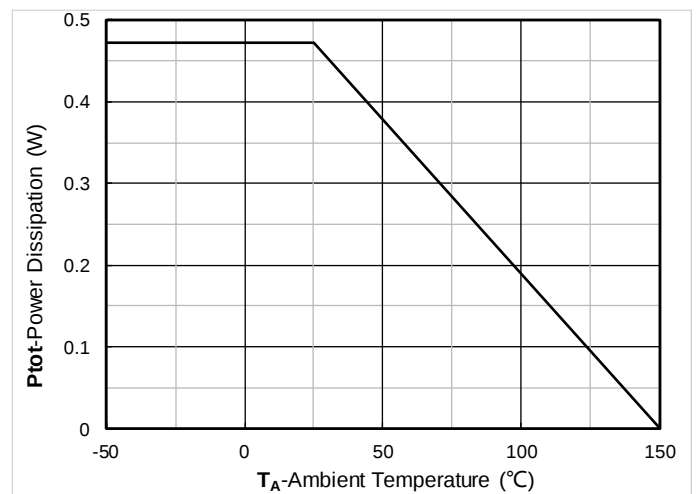


Figure 12. Power dissipation

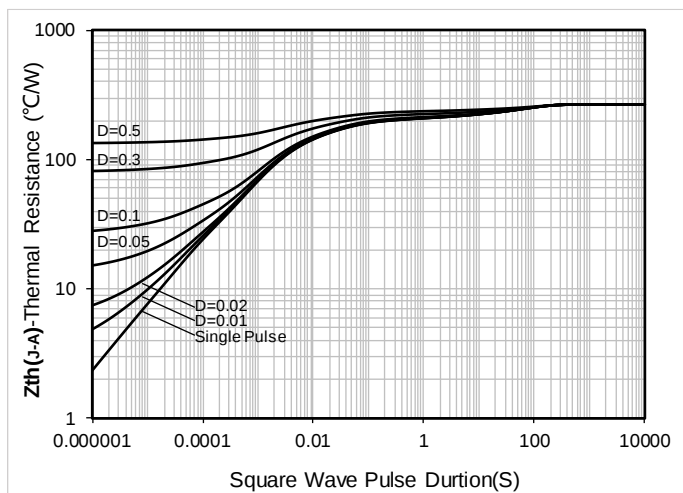


Figure 13. Maximum Transient Thermal Impedance

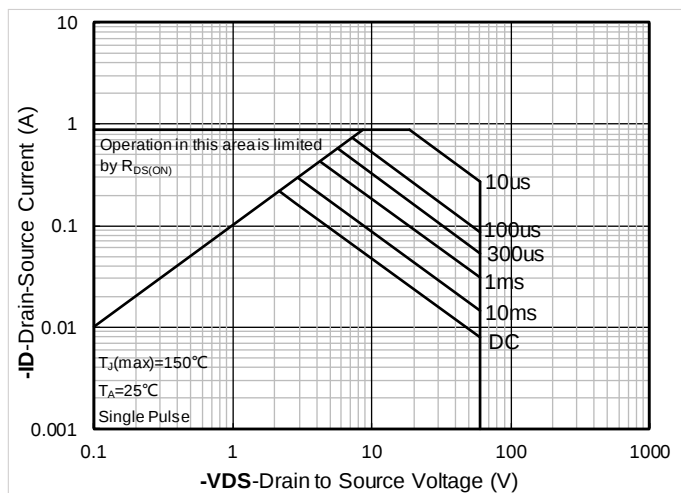
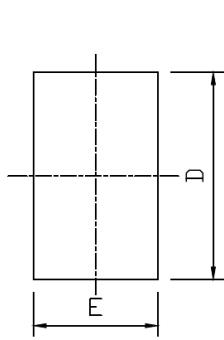


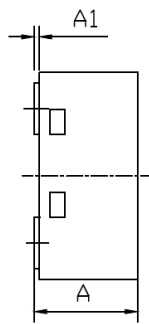
Figure 14. Safe Operation Area



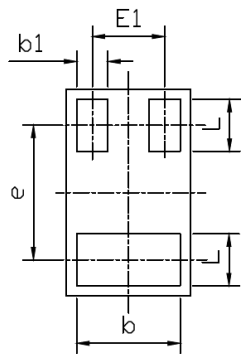
■ DFN1006-3L Package information



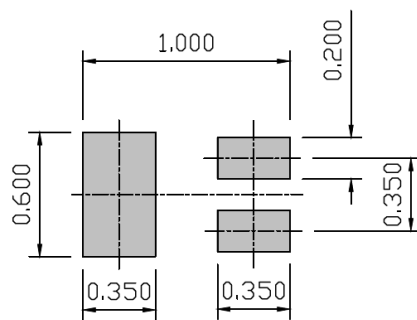
TOP VIEW



SIDE VIEW



BOTTOM VIEW



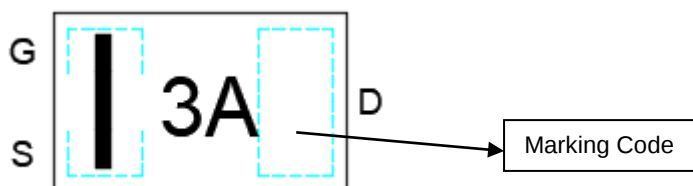
UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS		
	Millimeter		
	MIN.	NOM.	MAX.
A	0.30	---	0.45
A1	0.025REF		
b	0.45	0.50	0.55
b1	0.10	0.15	0.20
D	0.95	1.00	1.05
E	0.55	0.60	0.65
E1	0.35BSC		
e	0.65BSC		
L	0.20	0.25	0.30

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE LEAD BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

■ Marking Information**Note:**

1. All marking is at middle of the product body
2. All marking is in laser printing
3. 3A is marking code
4. Body color: Black



Disclaimer

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