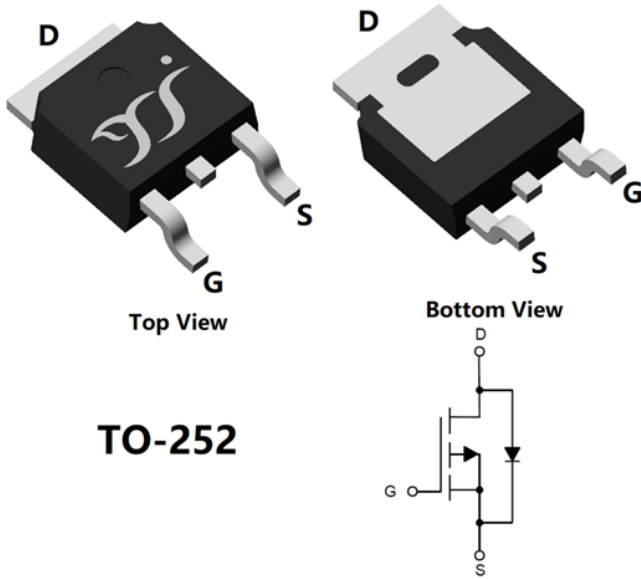


P-Channel Enhancement Mode Field Effect Transistor



Product Summary

• V_{DS}	-100V
• I_D	-46A
• $R_{DS(ON)}$ (at $V_{GS}=-10V$)	<34m Ω
• $R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	<42m Ω
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	
• ESD Level(HBM)	H3A

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- 48V Port

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-Source Voltage			V _{DS}	-	-100	V
Gate-Source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} =-10V	I _D	-	-6.1	A
		T _A =100°C,V _{GS} =-10V		-	-4.3	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} =-10V,Chip limitation		-	-46	
		T _C =100°C,V _{GS} =-10V		-	-32.5	
Pulsed Drain Current	T _C =25°C,t _p ≤10μs		I _{DM}	-	-184	
Maximum Body-Diode Continuous Current	T _C =25°C		I _S		-46	
Avalanche Energy (non-repetitive)	T _J =25°C,V _G =-10V,R _G =25Ω,L=0.5mH,I _{AS} =-30A		EAS	-	225	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	3	W
		T _A =100°C		-	1.5	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	166.6	
		T _C =100°C		-	83.3	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	175	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	50	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.9	



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■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A, T_J=25^\circ C$	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-100V, V_{GS}=0V, T_J=25^\circ C$	-	-	-1	μA
		$V_{DS}=-100V, V_{GS}=0V, T_J=125^\circ C$	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V, T_J=25^\circ C$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A, T_J=25^\circ C$	-1.3	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-25A, T_J=25^\circ C$	-	26	34	m Ω
		$V_{GS}=-4.5V, I_D=-13A, T_J=25^\circ C$	-	28	42	m Ω
Diode Forward Voltage	V_{SD}	$I_S=-25A, V_{GS}=0V, T_J=25^\circ C$	-	-0.84	-1.2	V
Gate Resistance	R_G	$f=1MHz, T_J=25^\circ C$	-	8	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=-50V, V_{GS}=0V, f=1MHz, T_J=25^\circ C$	-	5135	-	pF
Output Capacitance	C_{oss}		-	239	-	
Reverse Transfer Capacitance	C_{rss}		-	174	-	
Total Gate Charge	Q_g	$V_{GS}=-10V, V_{DS}=-50V, I_D=-25A, T_J=25^\circ C$	-	121.7	-	nC
Gate-Source Charge	Q_{gs}		-	16.9	-	
Gate-Drain Charge	Q_{gd}		-	23.7	-	
Output charge (Note 4)	Q_{oss}	$V_{DS}=-50V, V_{GS}=0V, T_J=25^\circ C$	-	19.8	-	nC
Reverse Recovery Charge	Q_{rr}	$I_F=-25A, di/dt=100A/\mu s, V_{GS}=0V, V_R=-50V, T_J=25^\circ C$	-	57	-	nC
Reverse Recovery Time	t_{rr}		-	34	-	ns
Turn-On Delay Time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-50V, I_D=-25A, R_{GEN}=3\Omega, T_J=25^\circ C$	-	12.4	-	ns
Turn-On Rise Time	t_r		-	36	-	
Turn-Off Delay Time	$t_{D(off)}$		-	174	-	
Turn-Off Fall Time	t_f		-	114	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $175^\circ C$. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■ Typical Electrical and Thermal Characteristics Diagrams

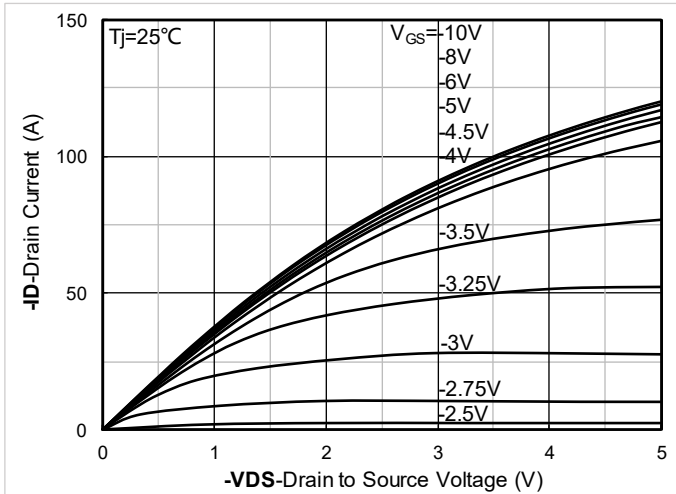


Figure 1. Output Characteristics; typical values

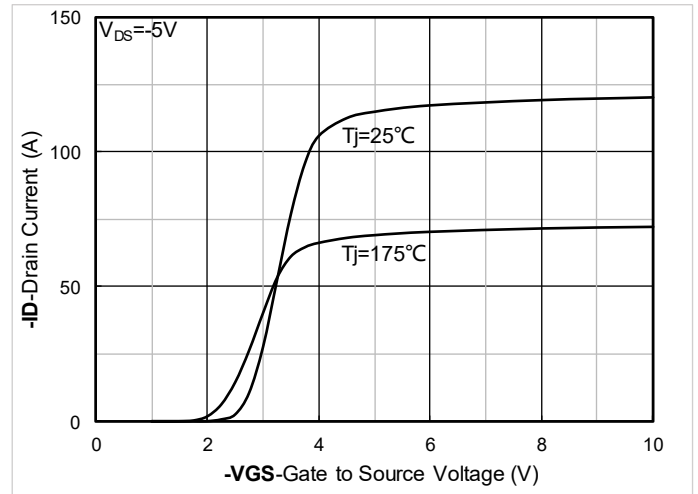


Figure 2. Transfer Characteristics; typical values

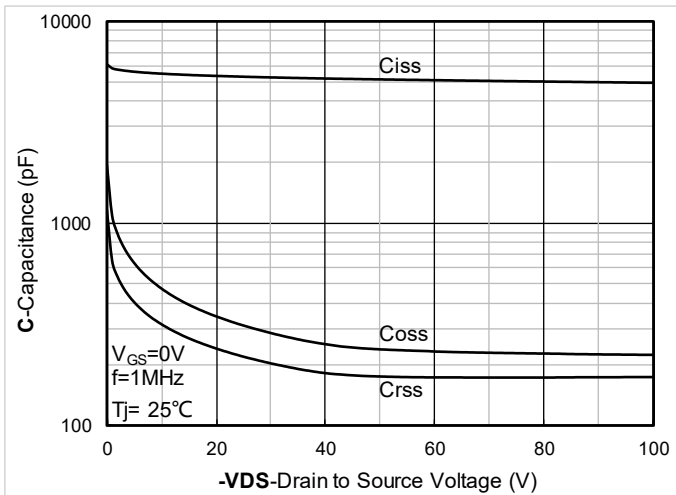


Figure 3. Capacitance Characteristics; typical values

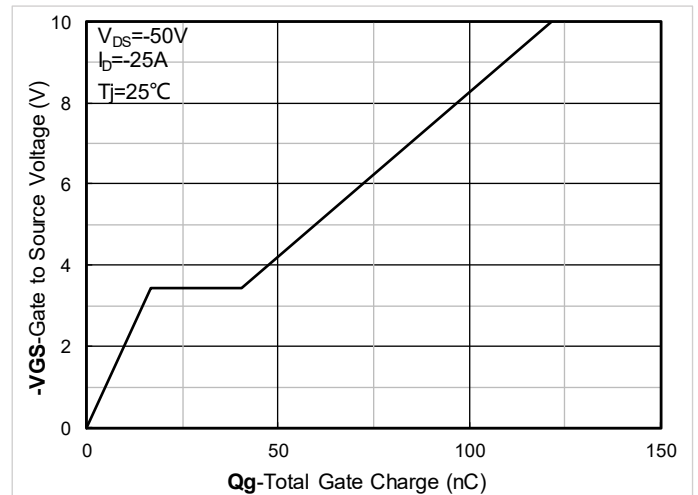


Figure 4. Gate Charge; typical values

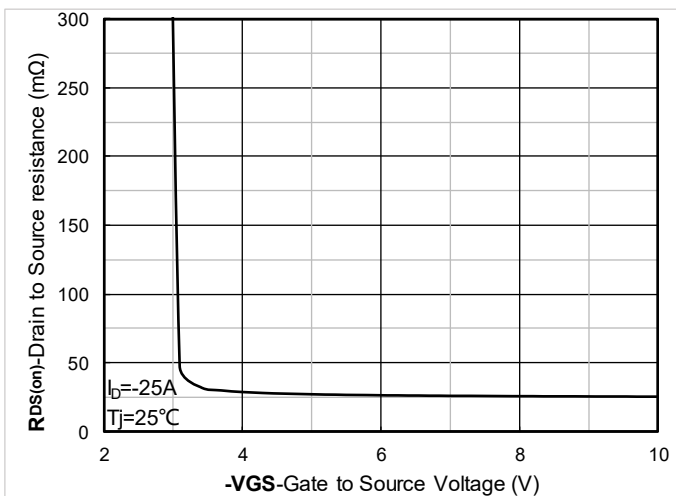


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

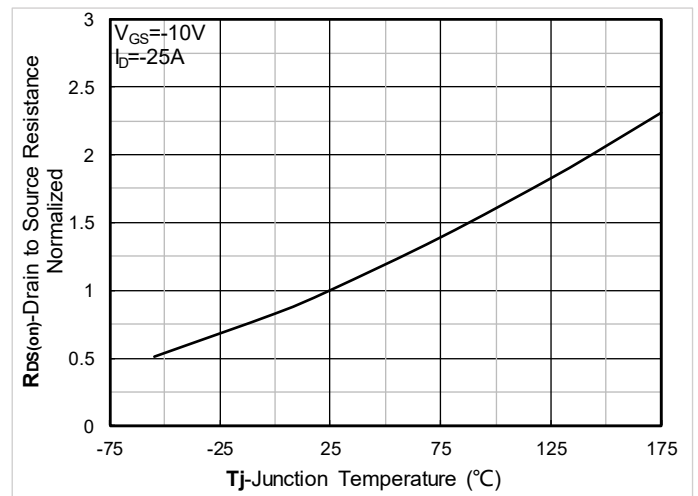


Figure 6. Normalized On-Resistance

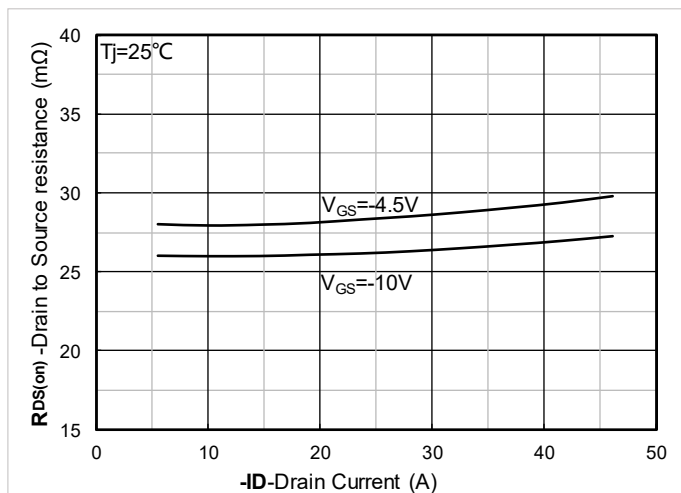


Figure 7. RDS(on) vs. Drain Current; typical values

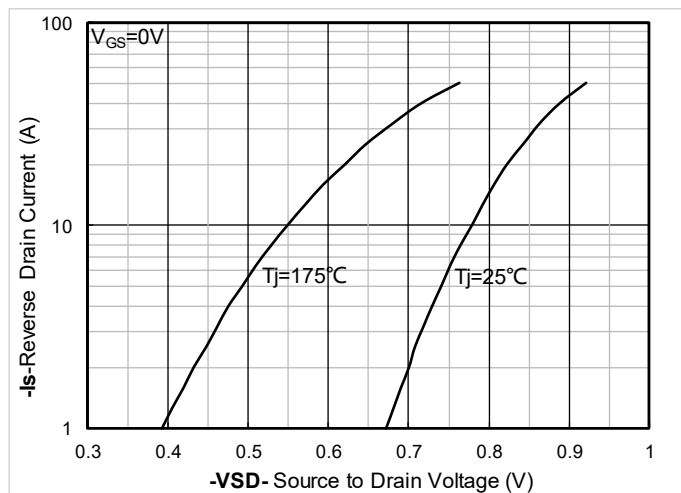


Figure 8. Forward characteristics of reverse diode; typical values

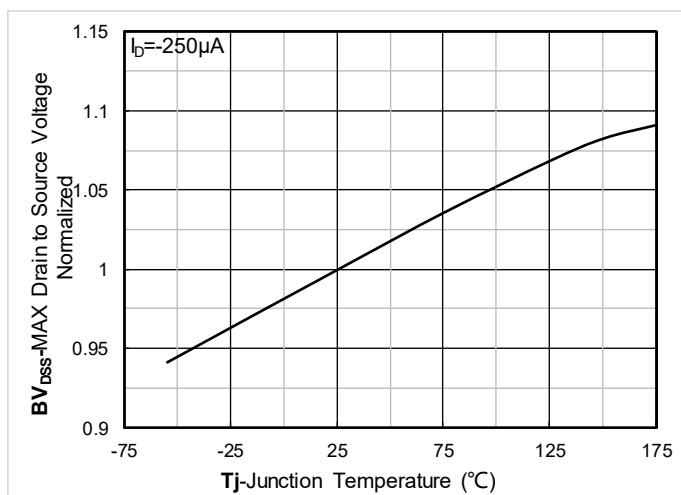


Figure 9. Normalized breakdown voltage

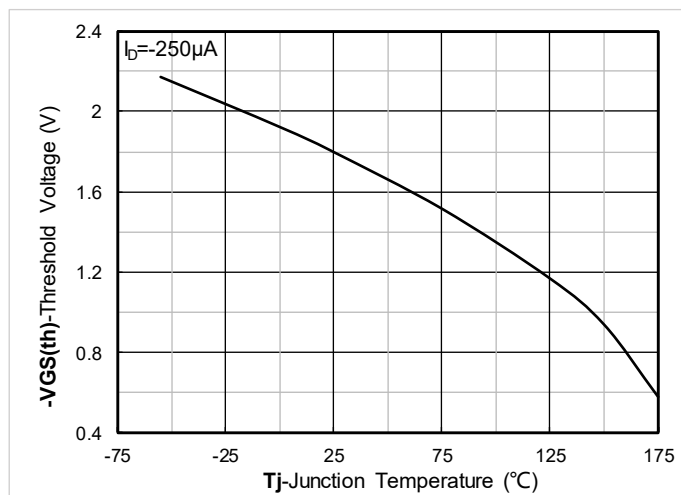


Figure 10. Gate Threshold voltage; typical values

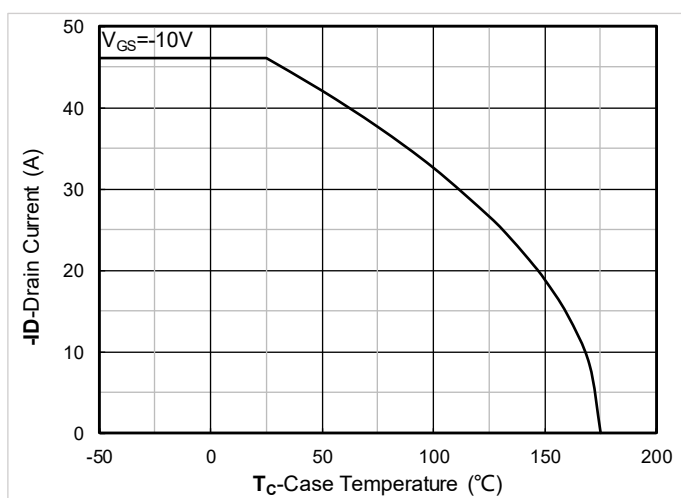


Figure 11. Current dissipation

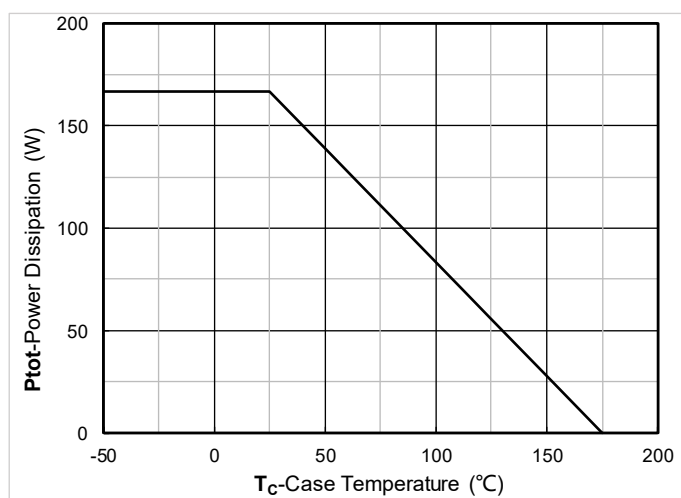


Figure 12. Power dissipation

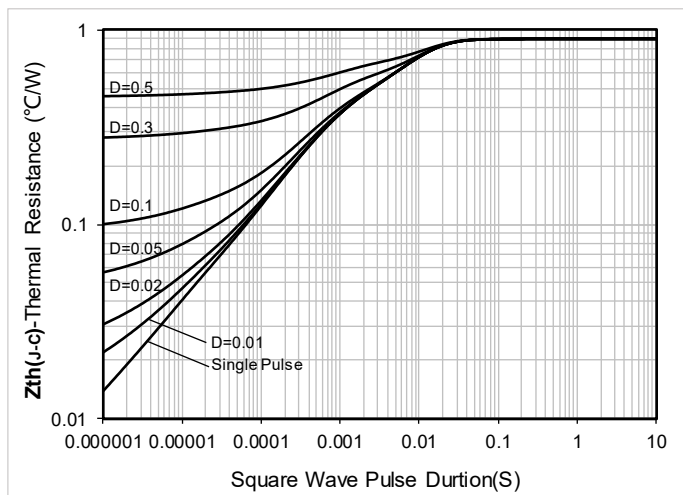


Figure 13. Maximum Transient Thermal Impedance

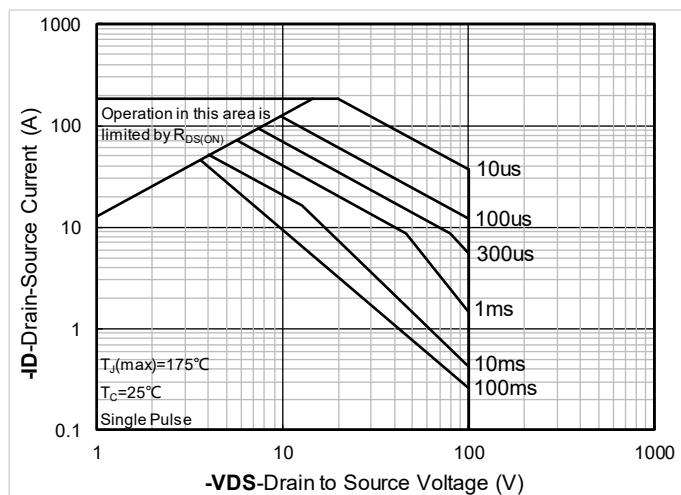
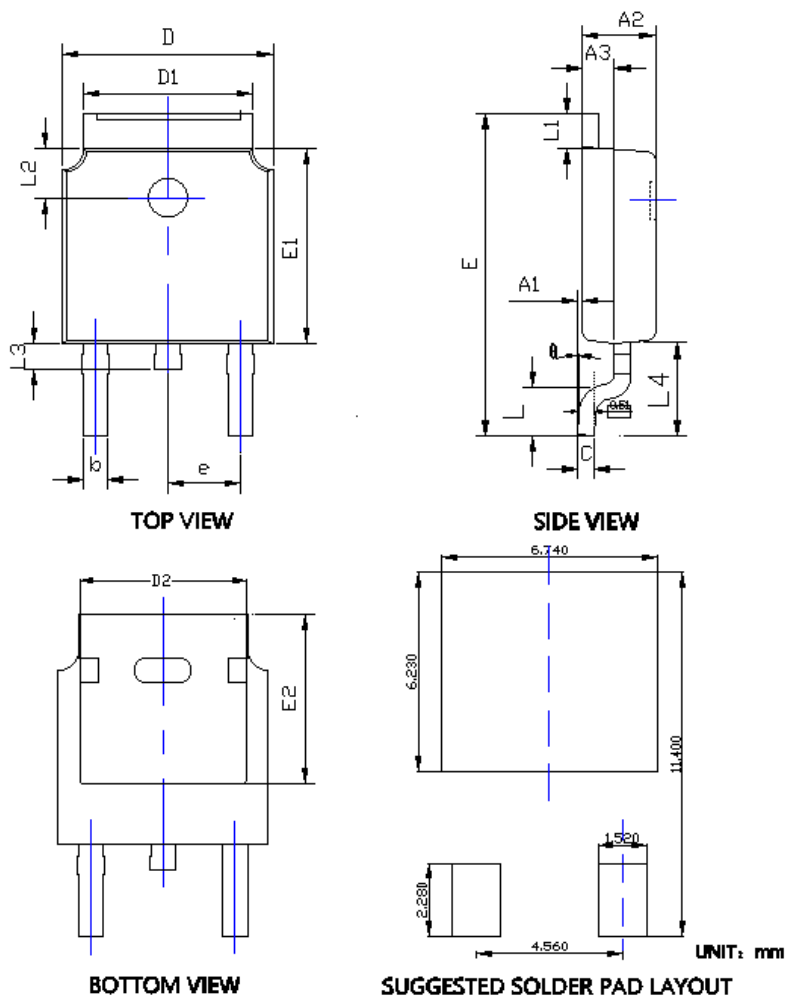


Figure 14. Safe Operation Area



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■ TO-252-F Package information



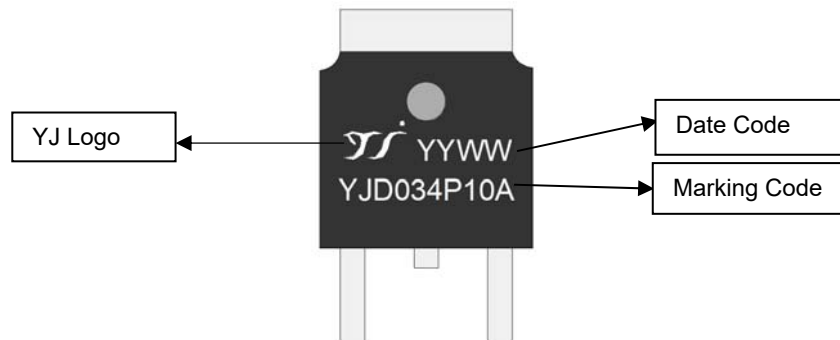
SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.197	0.205	0.213	5.000	5.200	5.400
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.024	0.031	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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