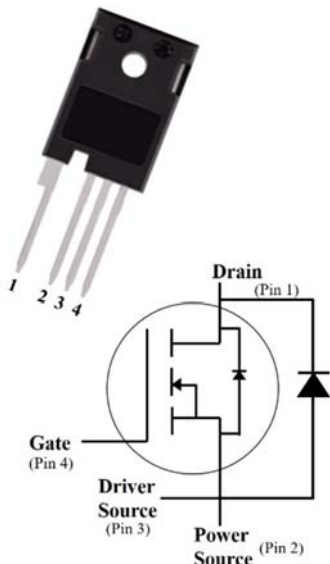


Silicon Carbide Power MOSFET (N-Channel Enhancement)

V_{DS}	750V
I_D (25°C)	58A
$R_{DS(on)}$	54mΩ



Features

- High speed switching
- Essentially no switching losses
- Reduction of heat sink requirements
- Maximum working temperature at 175 °C
- High blocking voltage
- Fast Intrinsic diode with low recovery current
- High-frequency operation
- Halogen free, RoHS compliant

Typical Applications

Typical applications are in power factor correction(PFC), solar inverter, uninterruptible power supply, motor drives, photovoltaic inverter, electric car and charger.

Mechanical Data

- Package: TO-247-4L
- Terminals: Tin plated leads
- Polarity: As marked

■Maximum Ratings ($T_c=25^\circ\text{C}$ Unless otherwise specified)

PARAMETER	SYMBOL	UNIT	VALUE	TEST CONDITIONS	NOTE
Device marking code			DH07570NCFYG3		
Drain source voltage @ $T_j=25^\circ\text{C}$	$V_{DS,max}$	V	750	$V_{GS}=0V$, $I_D=100\mu A$	
Gate source voltage @ $T_j=25^\circ\text{C}$	$V_{GS,max}$	V	-8/+22	Absolute maximum values (AC f > 1Hz, duty cycle < 1%)	
Gate source voltage @ $T_j=25^\circ\text{C}$	$V_{GS,op}$	V	-5/+18	Recommended operational values	
Continuous drain current @ $T_c=25^\circ\text{C}$	I_D	A	58	$V_{GS}=18V$, $T_c=25^\circ\text{C}$	Fig.17
Continuous drain current @ $T_c=100^\circ\text{C}$			42	$V_{GS}=18V$, $T_c=100^\circ\text{C}$	
Pulsed drain current	$I_{D(pulsed)}$	A	115	Pulse width t_p limited by $T_{j,max}^{(1)}$	Fig.22
Power Dissipation	P_{TOT}	W	238	$T_c=25^\circ\text{C}$	Fig.16
Power Dissipation			118	$T_c=100^\circ\text{C}$,	
Operating junction and Storage temperature range	T_j, T_{stg}	$^\circ\text{C}$	-55 to +175		
Soldering temperature	T_L	$^\circ\text{C}$	260	1.6mm (0.063") from case for 10s	
Mounting torque	T_M	Nm	0.6	M3 screw Maximum of mounting process: 3	

Note: (1) Typical Reference Conditions: $V_{GS} = V_{GS_on}$ PW < 10 μs , Duty cycle < 1%.



YJDH07570NCFYG3

■Static Electrical Characteristics (Tc=25°C unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Min.	Typ.	Max.	Test Conditions	Note
Gate threshold voltage	$V_{GS(th)}$	V	2.0	3.1	4.0	$V_{DS}=V_{GS}$, $I_D=8mA$	Fig.4, 11
				2.3		$V_{DS}=V_{GS}$, $I_D=8mA$, $T_J=175^\circ C$	
Drain source breakdown voltage	$V_{(BR)DSS}$	V	750			$V_{GS}=0V$, $I_D=100\mu A$	
Drain source leakage current	I_{DSS}	μA		10	100	$V_{DS}=750V$, $V_{GS}=0V$	
Gate source leakage current	I_{GSS}	nA		10	100	$V_{GS}=18V$, $V_{DS}=0V$	
Current drain source on-state resistance	$R_{DS\ ON}$	m Ω		70		$V_{GS}=15V$, $I_D=15A$	Fig.5, 6, 7
				54	70	$V_{GS}=18V$, $I_D=15A$	
				67		$V_{GS}=15V$, $I_D=15A$, $T_J=175^\circ C$	
				62		$V_{GS}=18V$, $I_D=15A$, $T_J=175^\circ C$	
Transconductance	g_f	S		16		$V_{DS}=20V$, $I_D=15A$	Fig.4
				15		$V_{DS}=20V$, $I_D=15A$, $T_J=175^\circ C$	

■Dynamic Electrical Characteristics (Tc=25°C unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Min.	Typ.	Max.	Test Conditions	Note
Input capacitance	C_{iss}	pF		1517		$V_{DS}=500V$, $V_{GS}=0V$, $T_J=25^\circ C$, $f=100KHz$, $V_{AC}=25mV$	Fig.13, 14
Output capacitance	C_{oss}			151			
Reverse capacitance	C_{rss}			7			
Coss stored energy	E_{oss}	μJ		21.3			Fig.15
Gate source charge	Q_{gs}	nC		19.5		$V_{DS}=500V$, $V_{GS}=-5/+18V$, $I_D=15A$	Fig.12
Gate drain charge	Q_{gd}			27.2			
Gate charge	Q_g			112			
Internal gate resistance	R_g	Ω		1.2		$f=1MHz$	

■Switching Characteristics (Tc=25°C unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Min.	Typ.	Max.	Test Conditions	Note
Turn on delay time	$t_{d(on)}$	ns		11.4		$V_{DD}=500V$, $V_{GS}=-5/+18V$, $I_D=15A$, $R_g=2.4\Omega$, $L=100\mu H$	Fig.21
Rise time	t_r			8.5			
Turn off delay time	$t_{d(off)}$	ns		17			
Fall time	t_f			10.4			
Turn on switching energy	E_{on}	μJ		41		$V_{DD}=500V$, $V_{GS}=-5/+18V$, $I_D=15A$, $R_g=2.4\Omega$, $L=100\mu H$	Fig.19, 20
Turn off switching energy	E_{off}			26			



■Body diode characteristics (T_c=25°C unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Min.	Typ.	Max.	Test Conditions	Note
Diode forward voltage	V _{SD}	V		0.8	1.5	V _{GS} =-5V, I _{SD} =7.5A	Fig.8
				0.5		V _{GS} =0V, I _{SD} =7.5A, T _j =175°C	Fig.9
Continuous diode forward current	I _S	A		49		V _{GS} =-5V, T _c =25°C	
Reverse recovery time	t _{rr}	nS		223		V _R =500V, V _{GS} =-5V, I _D =15A, di/dt=2150A/uS	
Reverse recovery charge	Q _{rr}	nC		8			
Peak reverse recovery current	I _{rrm}	A		59			

■Thermal Characteristics (T_a=25°C Unless otherwise specified)

SYMBOL	PARAMETER	UNIT	Typ.
R _{θJ-C}	Thermal Resistance from Junction to Case(SiC MOSFET)	°C /W	0.63
R _{θJ-C}	Thermal Resistance from Junction to Case(silicon FRD)	°C /W	0.51
R _{θJ-C}	Thermal Resistance from Junction to Case	°C /W	0.54

■Typical Characteristics

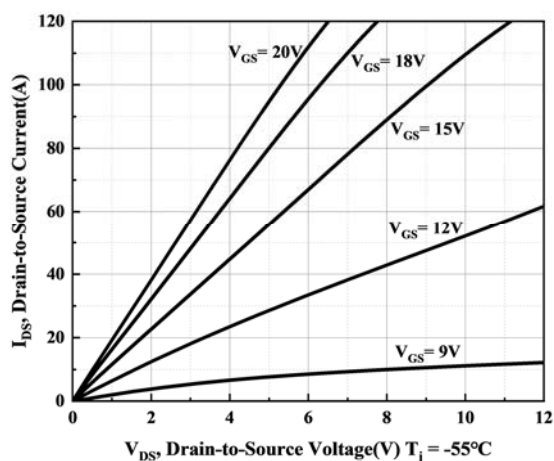


Figure 1. Output Characteristics T_j = -55°C

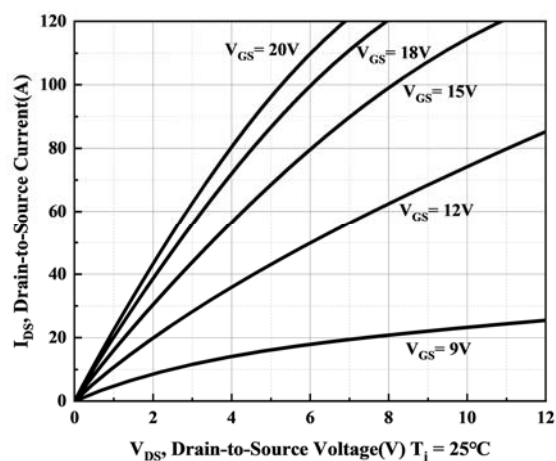


Figure2. Output Characteristics T_j = 25°C

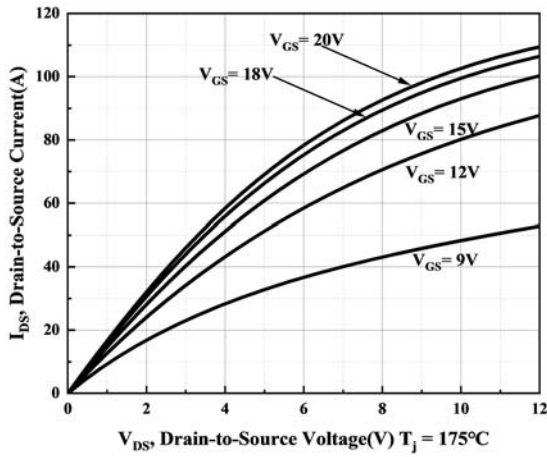


Figure 3. Output Characteristics $T_j = 175^\circ\text{C}$

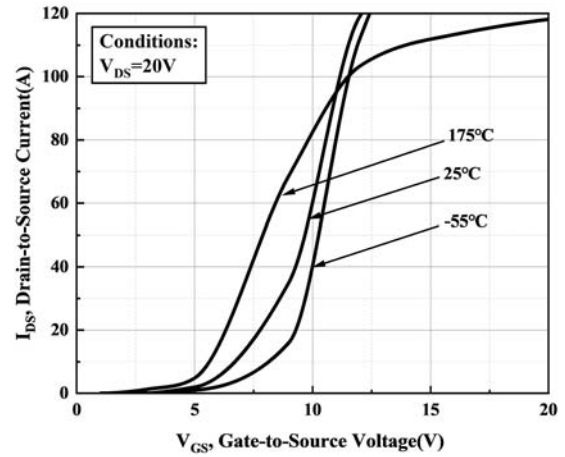


Figure 4. Transfer Characteristics for Various Junction Temperature

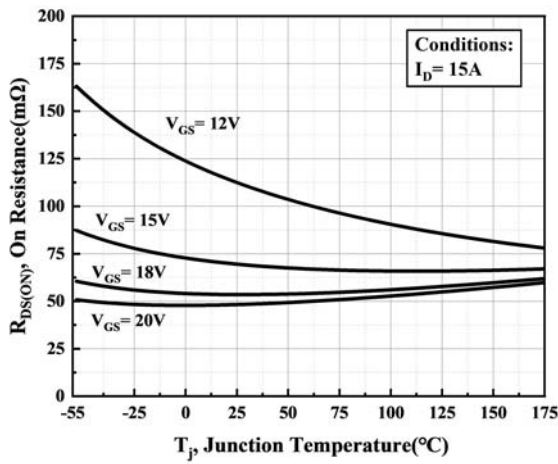


Figure 5. On-resistance vs. Temperature for Various Gate Voltage

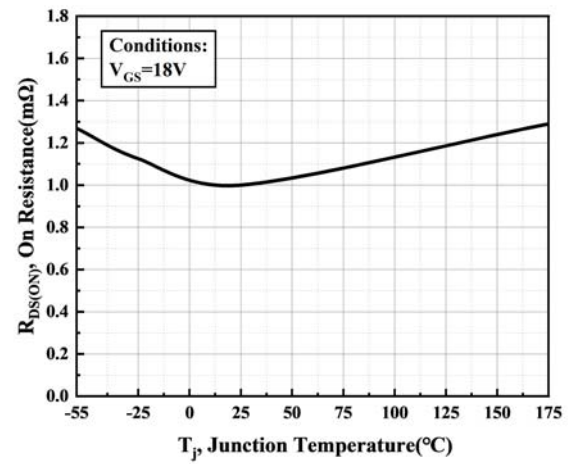


Figure 6. Normalized on-resistance vs. Temperature

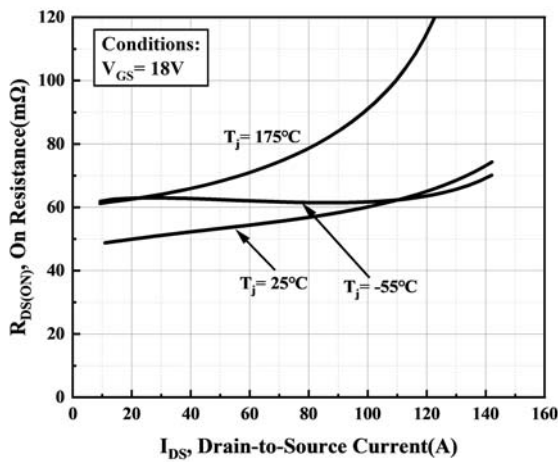


Figure 7. On-resistance vs. Drain Current

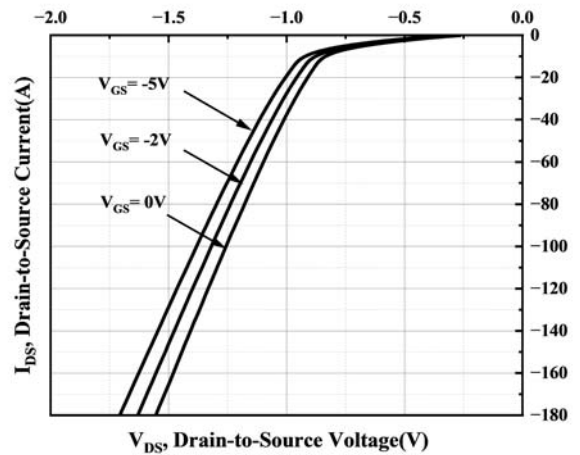


Figure 8. Reverse Characteristics at $T_j = 25^\circ\text{C}$

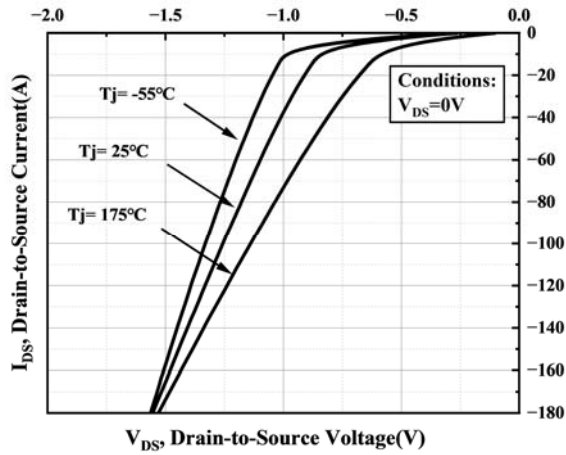


Figure 9. Reverse Characteristics

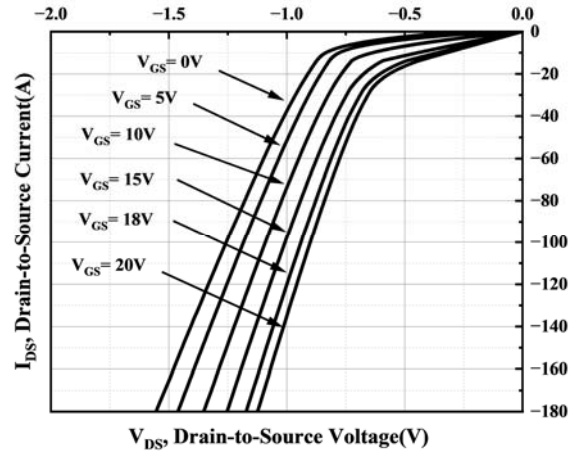


Figure 10. 3rd quadrant Characteristic at Tj= 25 °C

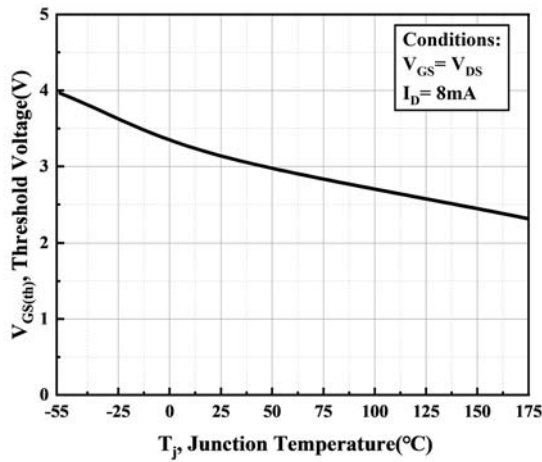


Figure 11. Threshold Voltage vs. Temperature

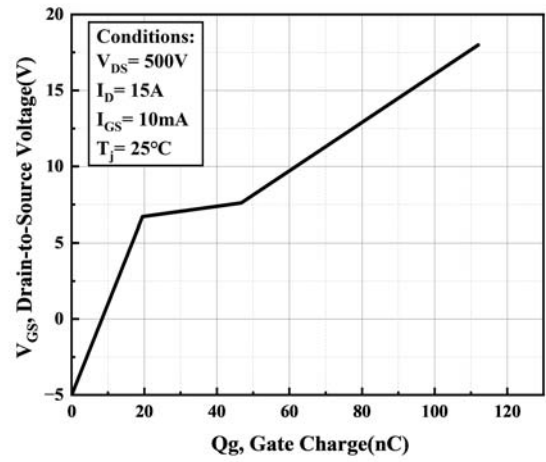


Figure 12. Gate Charge Characteristic

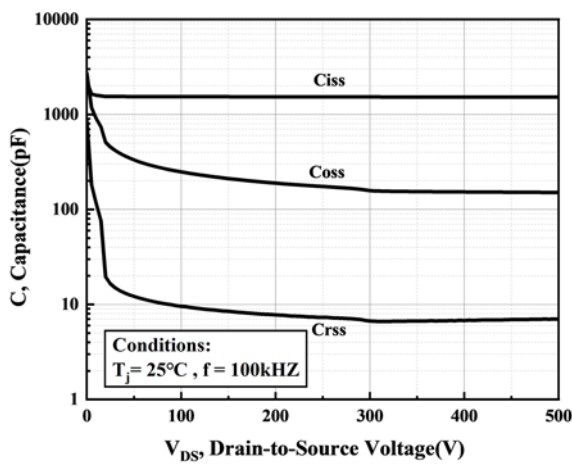


Figure 13. Capacitances vs. Drain Source Voltage (0-500V)

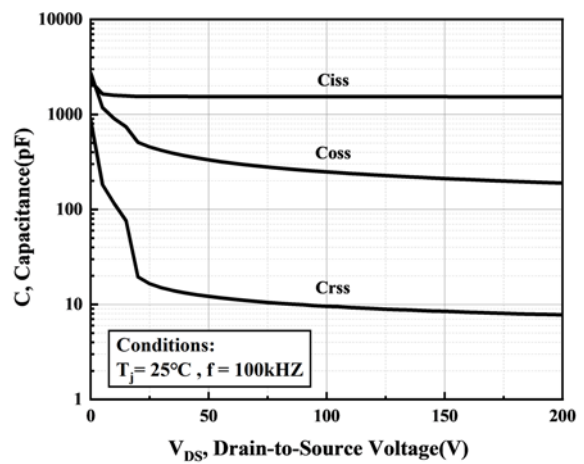


Figure 14. Capacitances vs. Drain Source Voltage (0-200V)

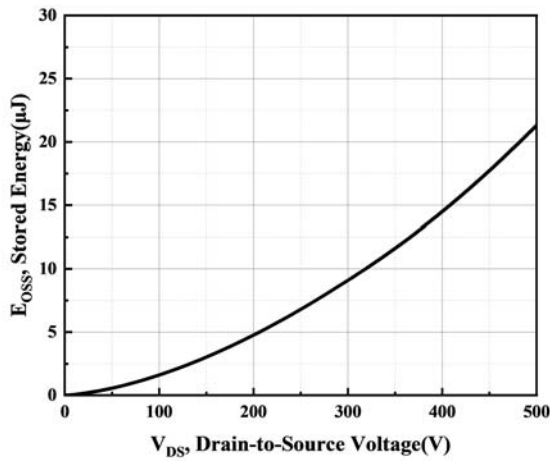


Figure 15. Output Capacitor Stored Energy

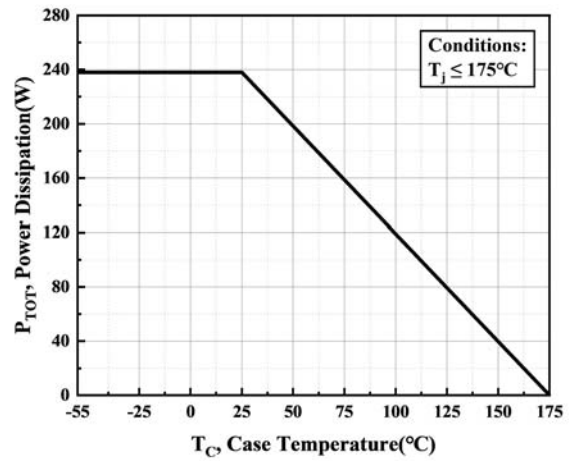


Figure 16. Maximum Power Dissipation Derating vs. Case Temperature

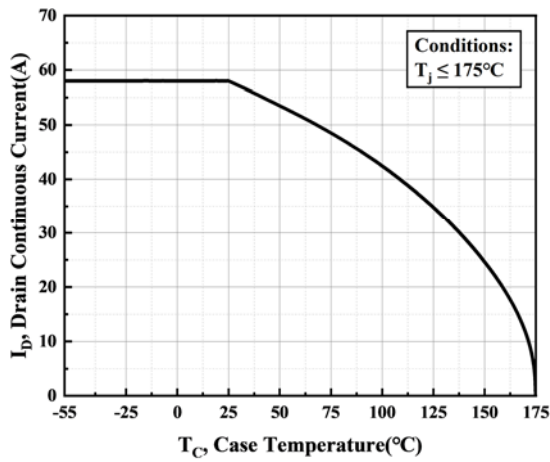


Figure 17. Continuous Drain Current Derating vs. Case Temperature

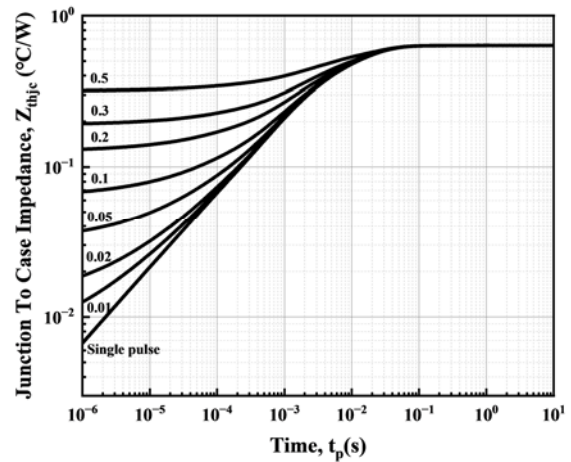


Figure18 Transient Thermal Impedance (MOSFET)

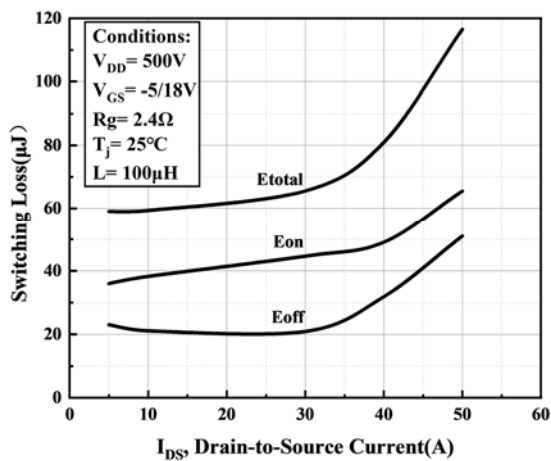


Figure 19. Clamped Inductive Switching Energy vs. Darin Current

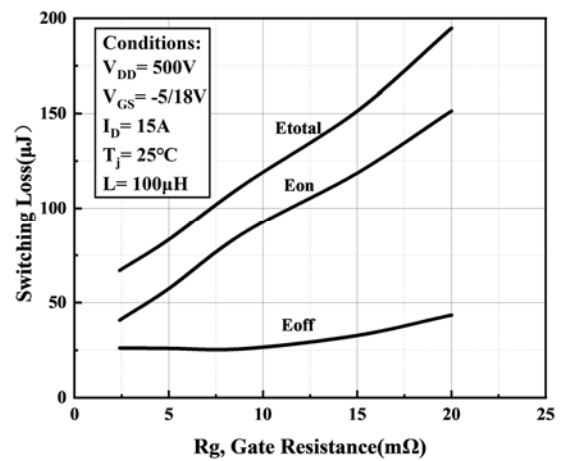


Figure 20. Clamped Inductive Switching Energy vs. Rg

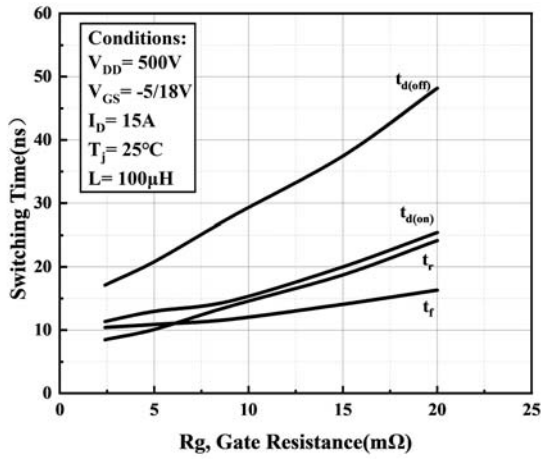


Figure 21. Switching Times vs. R_g

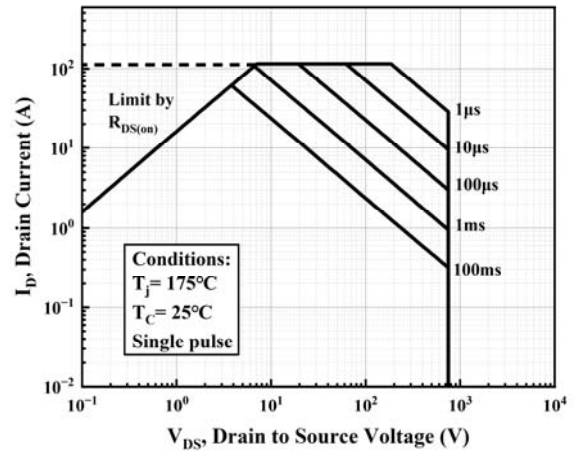


Figure 22. Safe Operating Area

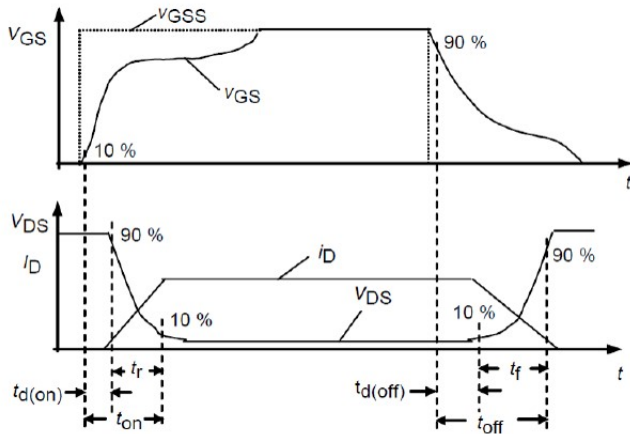


Figure 23. Switching Times Definition

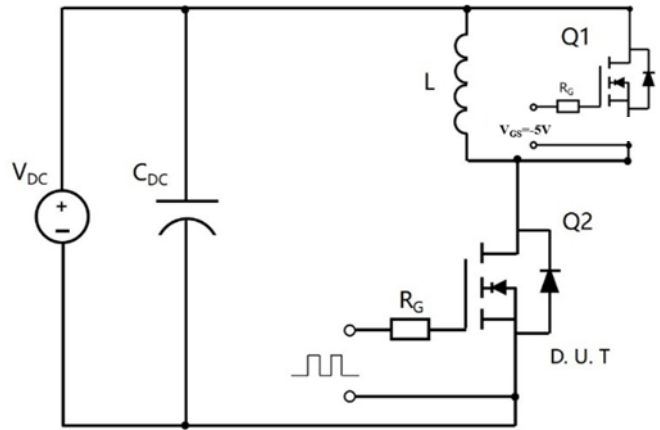
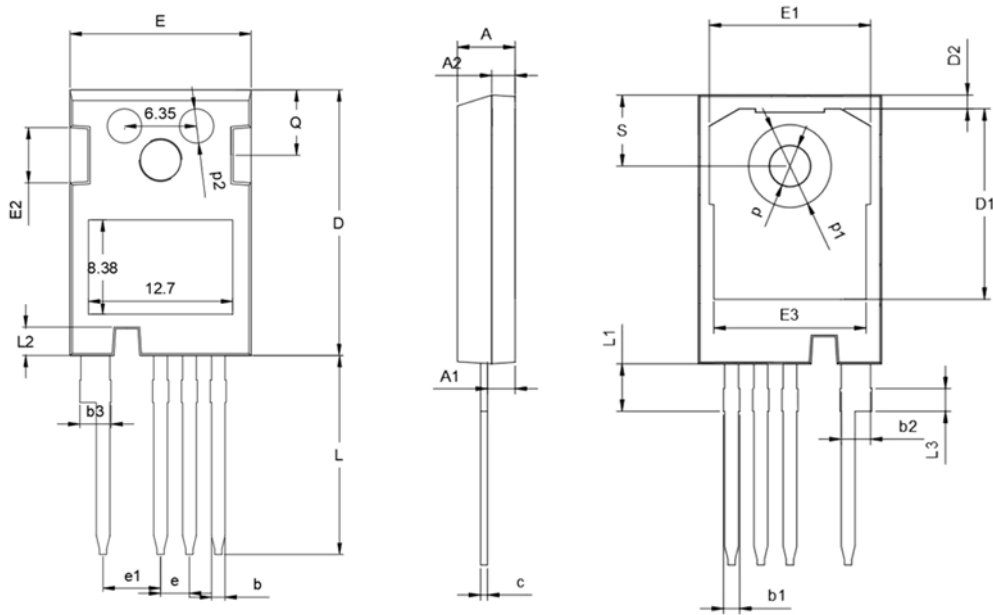


Figure 24. Clamped Inductive Switching Waveform Test Circuit

■Outline Dimensions



TO247-4L			
Dim	Min	Norm	Max
A	4.80	5.00	5.20
A1	2.30	2.40	2.50
A2	1.88	1.98	2.08
b	1.10	1.20	1.30
b1	1.20	/	1.50
b2	2.35	2.55	2.75
b3	2.45	/	2.85
c	0.55	0.60	0.65
D	23.3	23.45	23.6
D1	16.25	16.55	16.85
D2	1.00	/	1.30
e	TYP2.54		
e1	TYP5.06		
E	15.75	15.90	16.05
E1	13.80	/	14.20
E2	4.40	4.75	5.10
E3	13.00	/	13.45
L	17.34	17.49	17.64
L1	4.00	/	4.30
L2	2.35	/	2.65
L3	TYP1.98		
Q	5.60	5.80	6.00
S	6.05	/	6.30
p	TYP3.58		
p1	TYP7.18		
p2	TYP3.00		



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