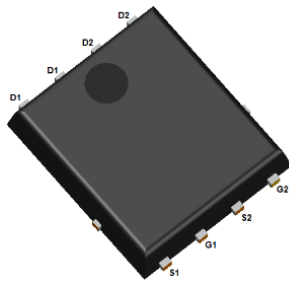
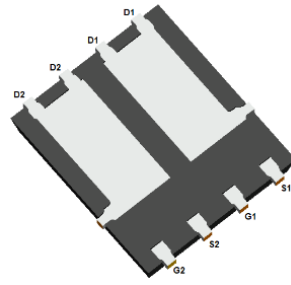


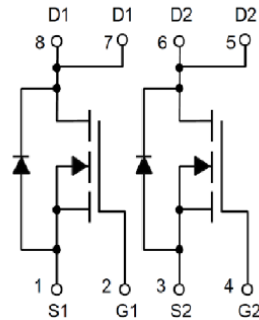
N-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View



PDFN5060-8L

Product Summary

NMOS(Die1/Die2)

- V_{DS} 60V
- I_D 50A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 10 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 15 mohm
- ESD Rating Up to 250V(HBM)

General Description

- Split gate trench MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application
- 12V, 24V Automotive systems

■ Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	N-Die1/Die2	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^{\circ}C$	I_D	50	A
	$T_C=100^{\circ}C$		31	
	$T_A=25^{\circ}C$		12	
	$T_A=100^{\circ}C$		7	
Pulsed Drain Current ^A		I_{DM}	150	A
Avalanche energy ^B		EAS	162	mJ
Total Power Dissipation ^C	$T_C=25^{\circ}C$	P_D	69	W
	$T_C=100^{\circ}C$		27	
	$T_A=25^{\circ}C$		2.5	
	$T_A=100^{\circ}C$		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^{\circ}C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	40	50	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.5	1.8	



YJGD50G06AQ

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD50G06AQ	F1	YJGD50G06A	5000	10000	100000	13" reel

■ NMOS(Die1/Die2) Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A		6.5	10	mΩ
		V _{GS} = 4.5V, I _D =10A		8.5	15	
Diode Forward Voltage	V _{SD}	I _S =20A,V _{GS} =0V		0.85	1.2	V
Gate Resistance	R _g	f=1MHz		1.5		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V,f=1MHZ		2100		pF
Output Capacitance	C _{oss}			630		
Reverse Transfer Capacitance	C _{rss}			33		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =20A	-	31	-	nC
Gate-Source Charge	Q _{gs}		-	6	-	
Gate-Drain Charge	Q _{gd}		-	5	-	
Reverse Recovery Chrage	Q _{rr}	I _F =20A, di/dt=500A/us	-	18	-	ns
Reverse Recovery Time	t _{rr}		-	30	-	
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V, I _D =20A R _{GEN} =3Ω	-	10	-	
Turn-on Rise Time	t _r		-	34	-	
Turn-off Delay Time	t _{D(off)}		-	26.2	-	
Turn-off fall Time	t _f		-	45	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=1mH, I_{AS}=18A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



■ NMOS(Die1/Die2) Typical Performance Characteristics

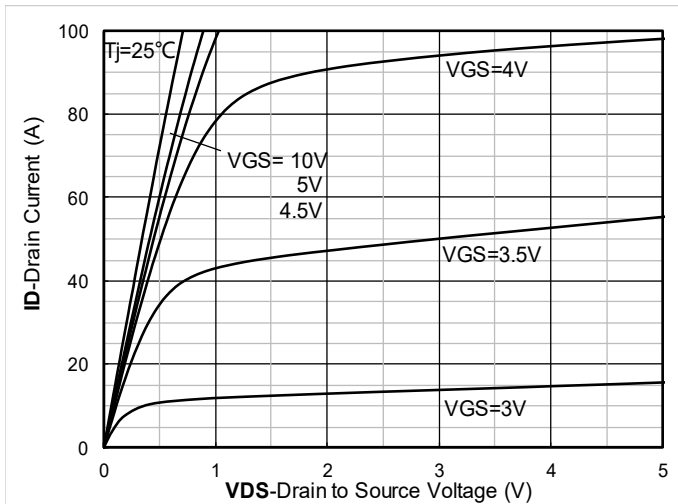


Figure1. Output Characteristics

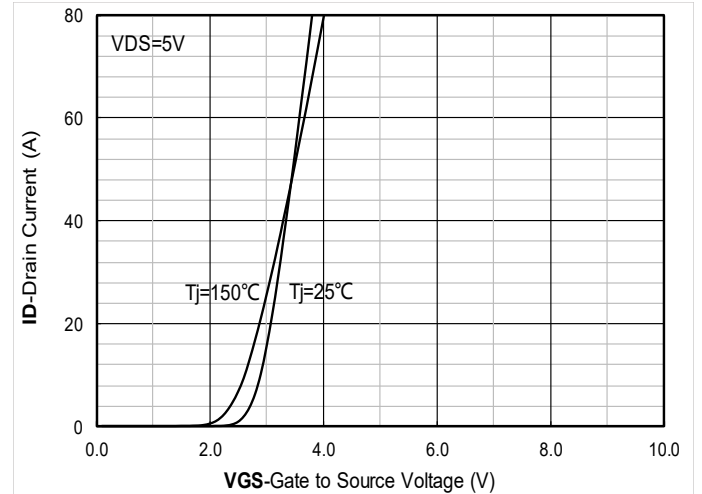


Figure2. Transfer Characteristics

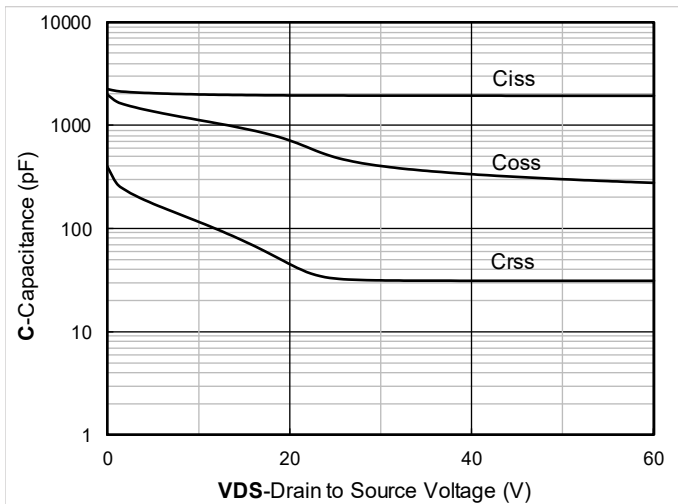


Figure3. Capacitance Characteristics

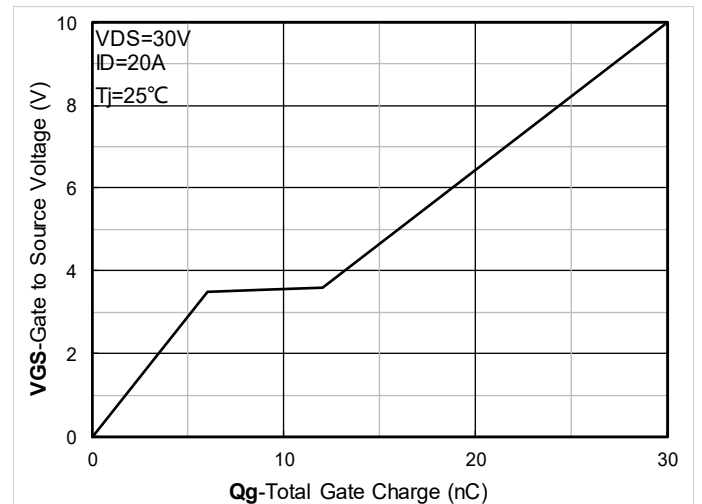


Figure4. Gate Charge

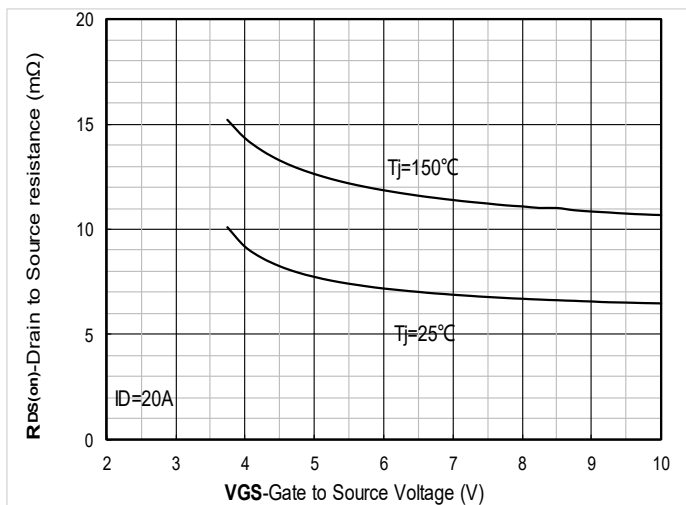


Figure5. On-Resistance vs. Gate to Source Voltage

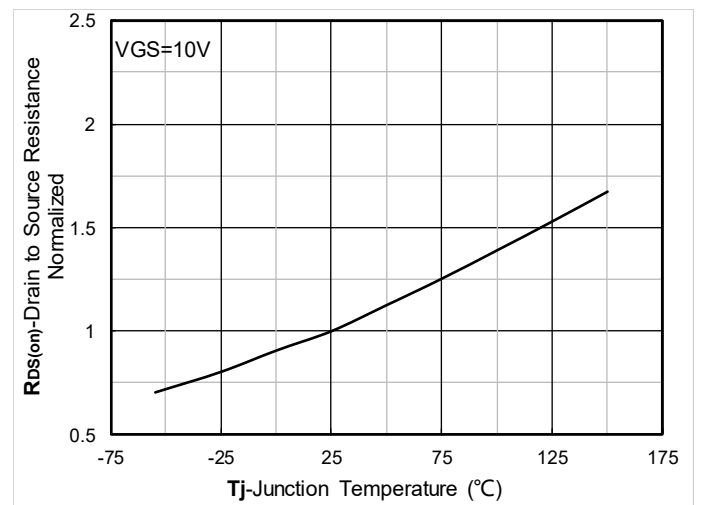


Figure6. Normalized On-Resistance

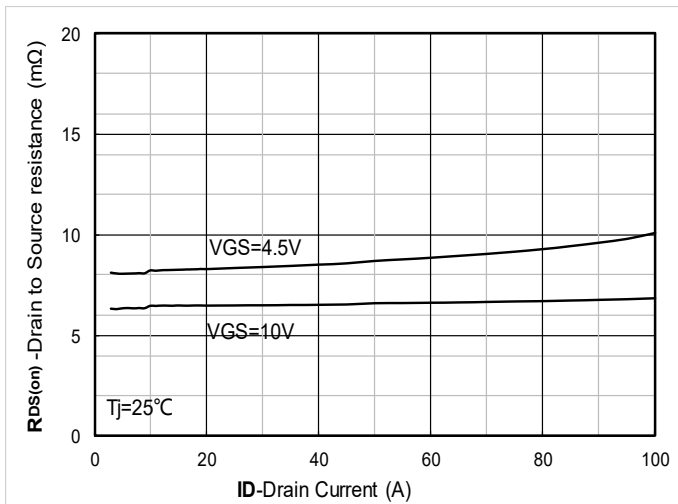


Figure 7. $R_{DS(on)}$ VS Drain Current

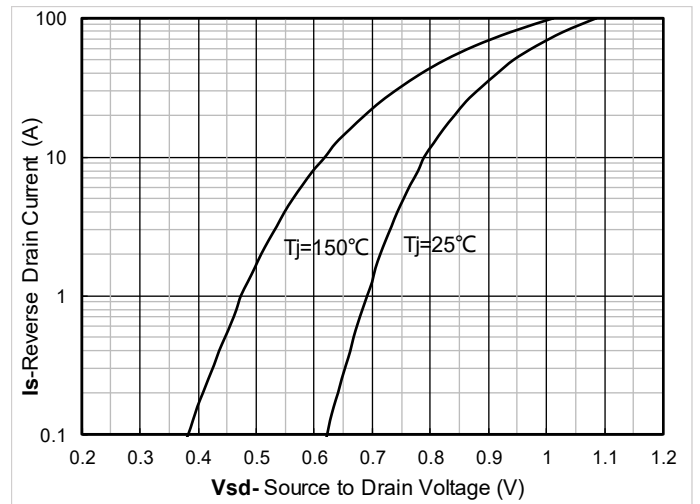


Figure 8. Forward characteristics of reverse diode

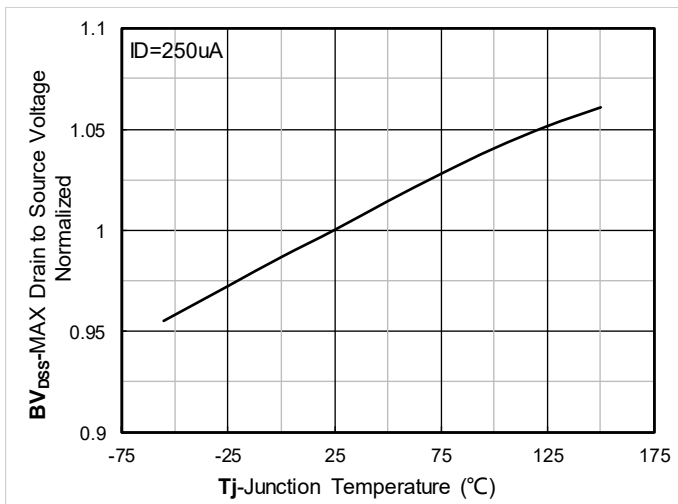


Figure 9. Normalized breakdown voltage

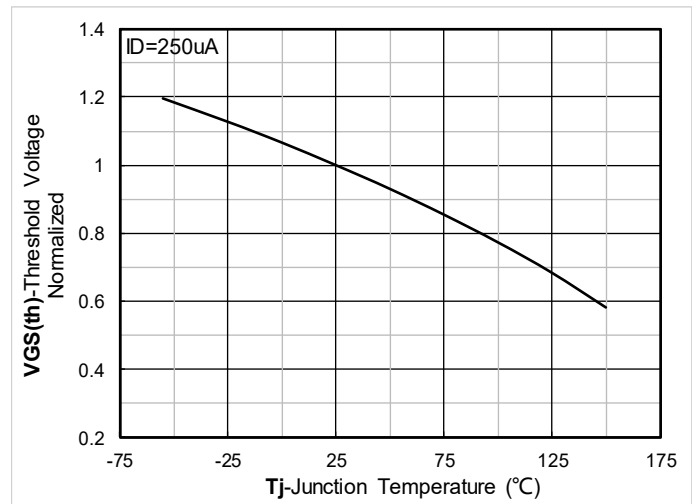


Figure 10. Normalized Threshold voltage

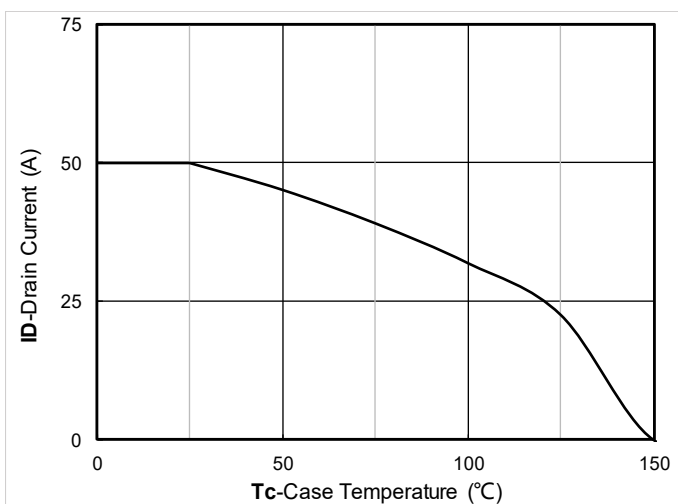


Figure 11. Current dissipation

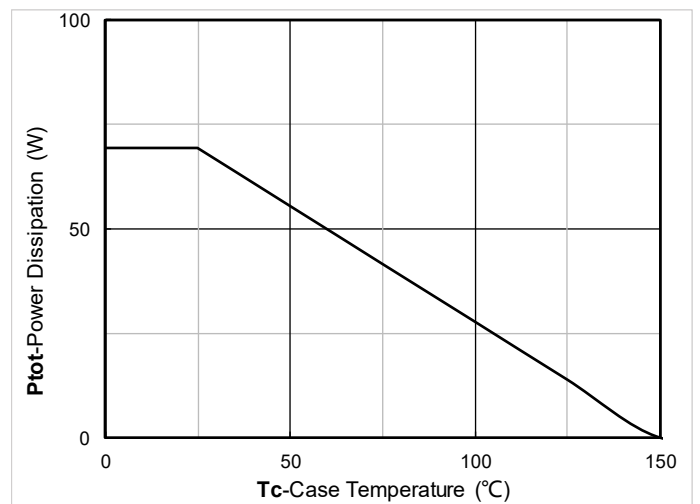


Figure 12. Power dissipation

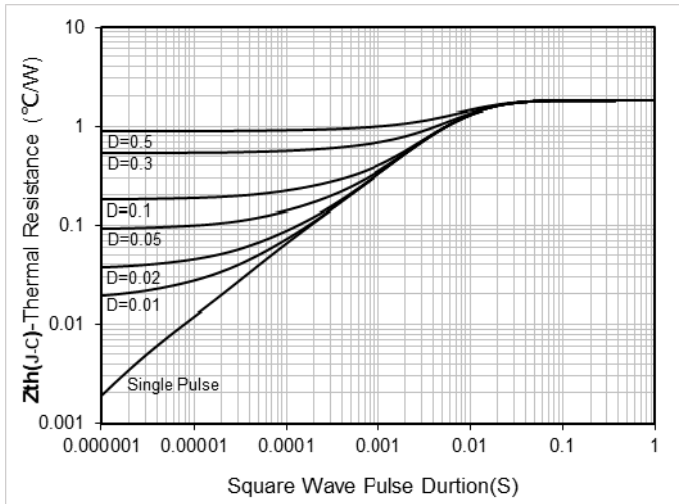


Figure 13. Maximum Transient Thermal Impedance

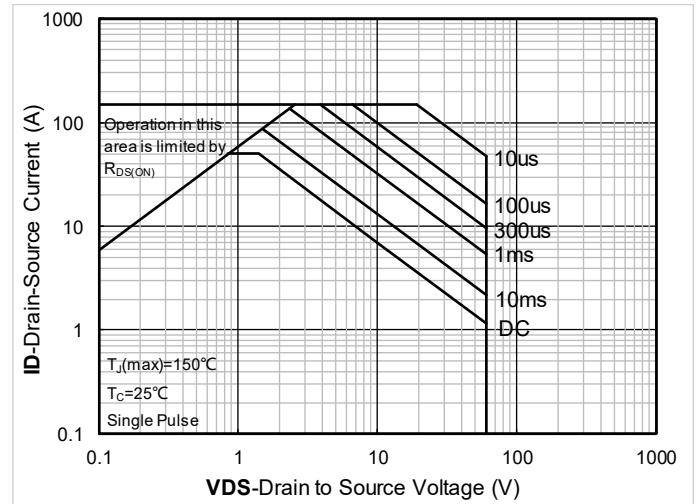
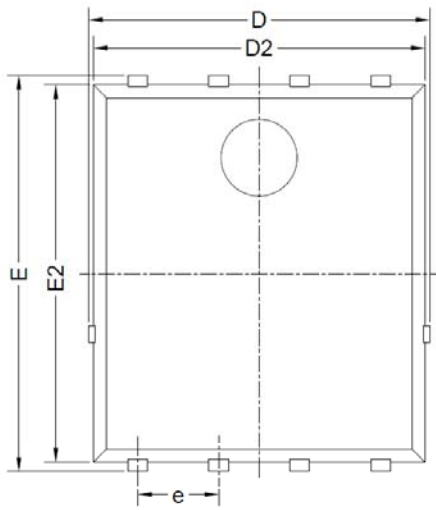


Figure 14. Safe Operation Area

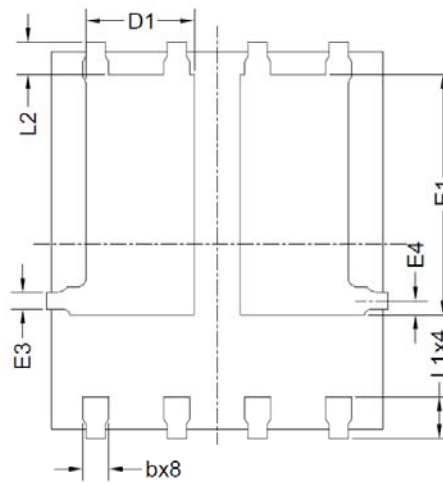


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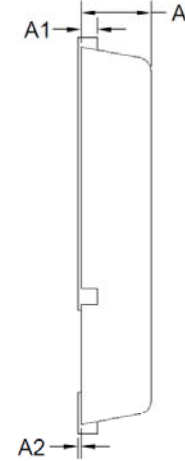
■ PDFN5060-8L Package information



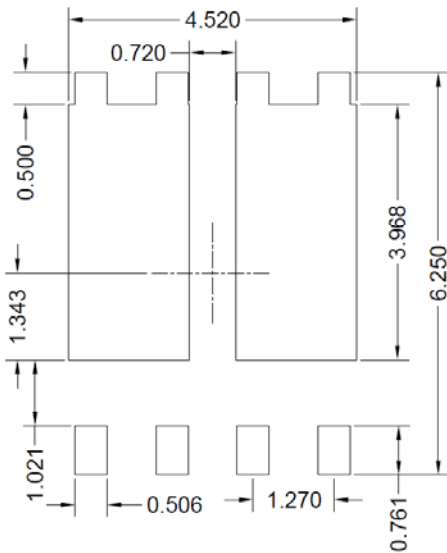
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254REF		
E4	0.21REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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