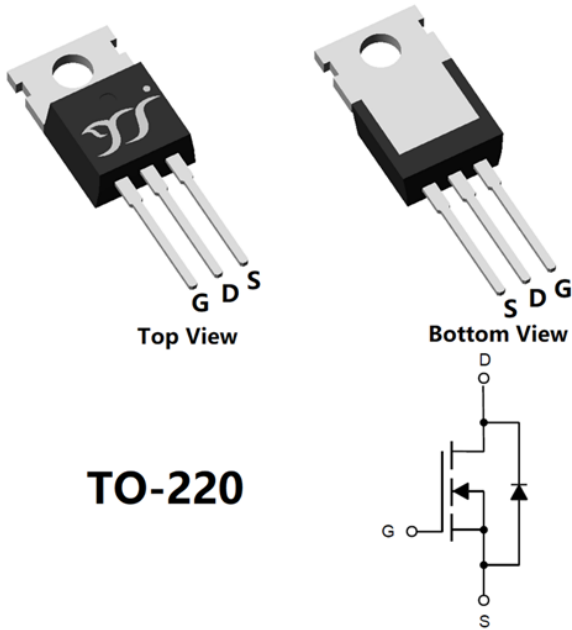




N-Channel Enhancement Mode Field Effect Transistor



Product Summary

• V_{DS}	150V
• I_D	74A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	$<11.4m\Omega$
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	$<16.2m\Omega$
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	
• ESD Level(HBM)	H2

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	150	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} = 10V	I _D	-	12.1	A
		T _A =100°C,V _{GS} = 10V		-	7.6	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} = 10V,Chip limitation		-	74	
		T _C =100°C,V _{GS} = 10V		-	46.8	
Pulsed Drain Current	T _C =25°C,t _p ≤10μs		I _{DM}	-	296	
Maximum Body-Diode Continuous Current	T _C =25°C		I _S		74	
Avalanche Energy (non-repetitive)	T _J =25°C,V _G =10V,R _G =25Ω,L=0.5mH,I _{AS} =32.2A		EAS	-	259.2	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	3.67	W
		T _A =100°C		-	1.47	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	138.8	
		T _C =100°C		-	55.5	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	150	°C

■ Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	34	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.9	



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■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A, T_j=25^\circ C$	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=150V, V_{GS}=0V, T_j=25^\circ C$	-	-	1	μA
		$V_{DS}=150V, V_{GS}=0V, T_j=125^\circ C$	-	-	100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V, T_j=25^\circ C$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A, T_j=25^\circ C$	1.2	1.95	2.8	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A, T_j=25^\circ C$	-	9.5	11.4	m Ω
		$V_{GS}=4.5V, I_D=20A, T_j=25^\circ C$	-	10.8	16.2	m Ω
Diode Forward Voltage	V_{SD}	$I_S=50A, V_{GS}=0V, T_j=25^\circ C$	-	0.91	1.2	V
Gate Resistance	R_G	$f=1MHz, T_j=25^\circ C$	-	0.8	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=75V, V_{GS}=0V, f=1MHz, T_j=25^\circ C$	-	3416	-	pF
Output Capacitance	C_{oss}		-	275	-	
Reverse Transfer Capacitance	C_{rss}		-	9.4	-	
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=75V, I_D=50A, T_j=25^\circ C$	-	48.6	-	nC
Gate-Source Charge	Q_{gs}		-	10.9	-	
Gate-Drain Charge	Q_{gd}		-	7.5	-	
Reverse Recovery Charge	Q_{rr}	$I_F=50A, di/dt=100A/\mu s, V_{GS}=0V, V_R=75V, T_j=25^\circ C$	-	185	-	nC
Reverse Recovery Time	t_{rr}		-	84	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=75V, I_D=50A, R_{GEN}=3\Omega, T_j=25^\circ C$	-	14	-	ns
Turn-on Rise Time	t_r		-	8.4	-	
Turn-off Delay Time	$t_{D(off)}$		-	36	-	
Turn-off Fall Time	t_f		-	10.6	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■ Typical Electrical and Thermal Characteristics Diagrams

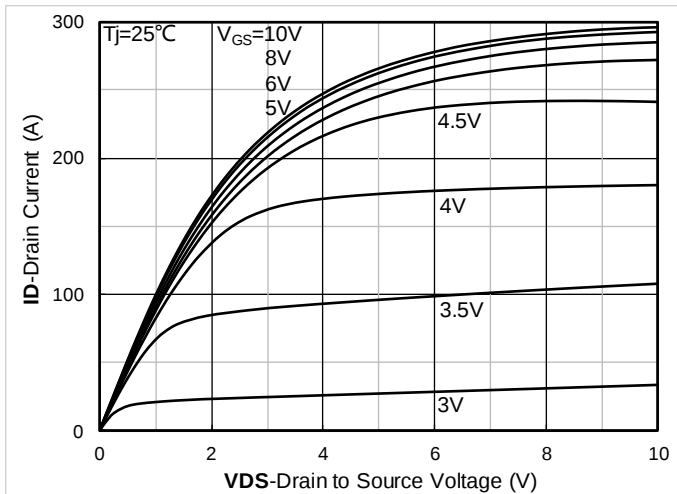


Figure 1. Output Characteristics; typical values

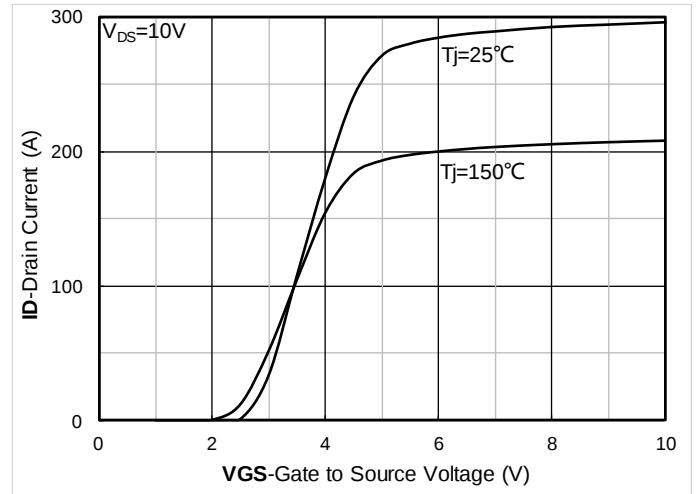


Figure 2. Transfer Characteristics; typical values

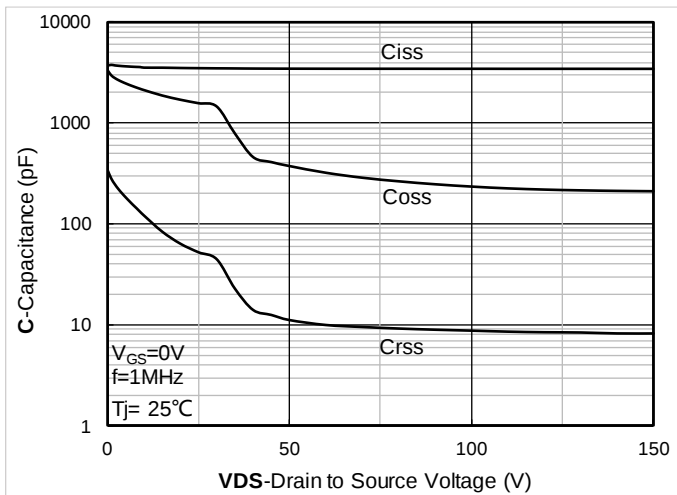


Figure 3. Capacitance Characteristics; typical values

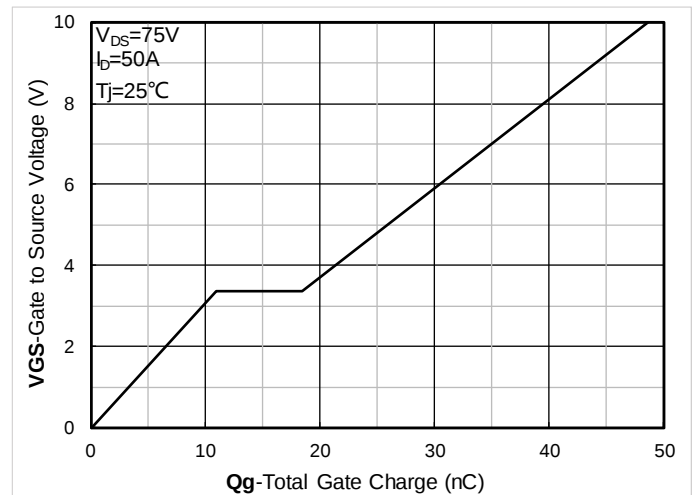


Figure 4. Gate Charge; typical values

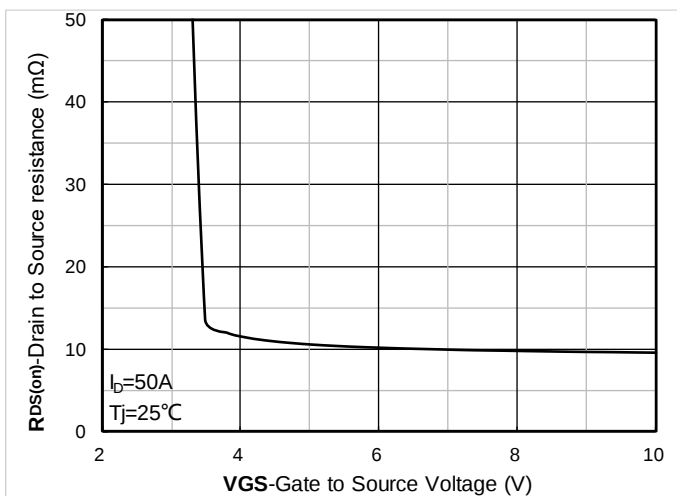


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

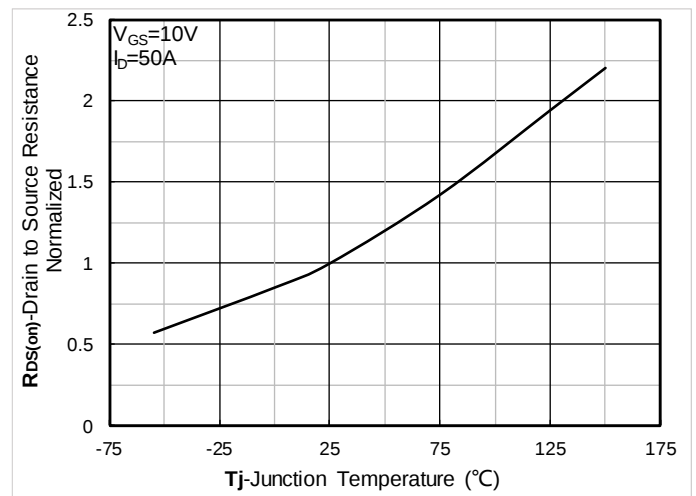


Figure 6. Normalized On-Resistance

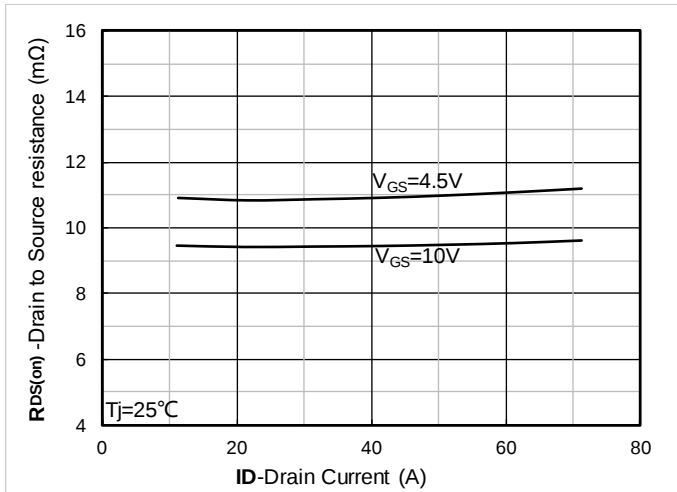


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

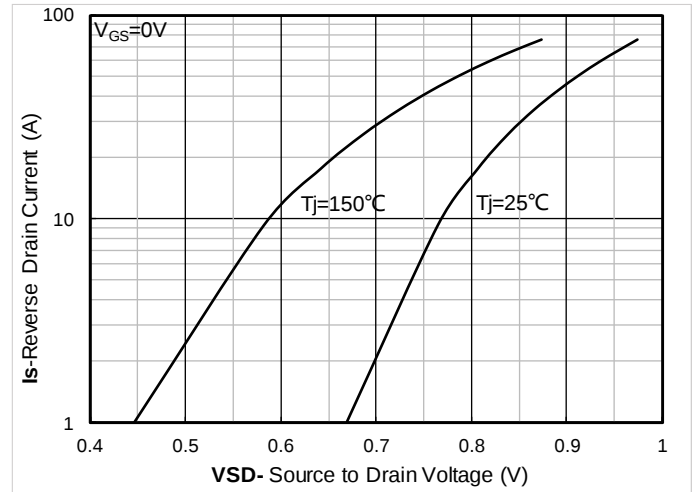


Figure 8. Forward characteristics of reverse diode; typical values

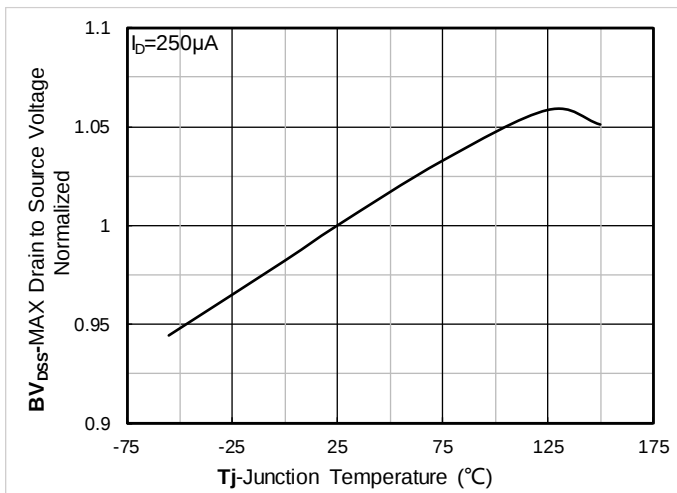


Figure 9. Normalized breakdown voltage

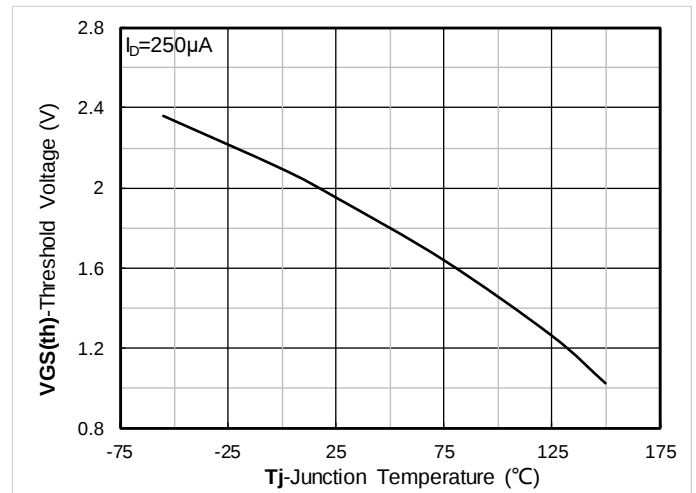


Figure 10. Gate Threshold voltage; typical values

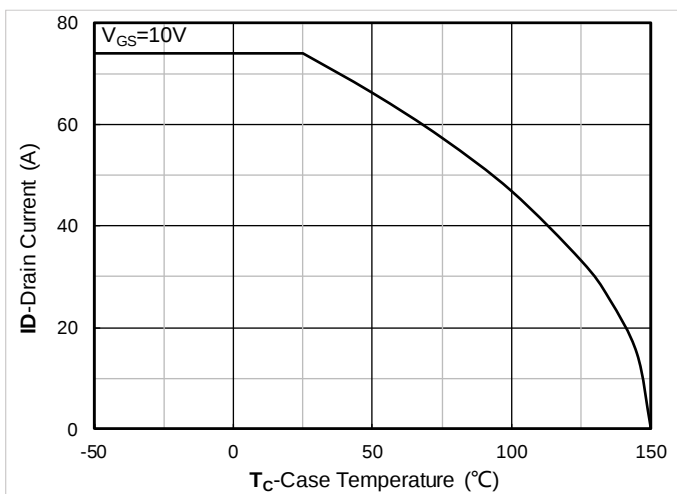


Figure 11. Current dissipation

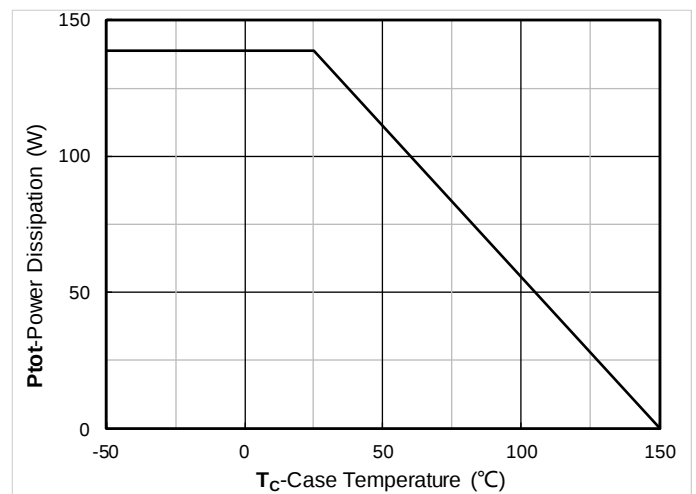


Figure 12. Power dissipation

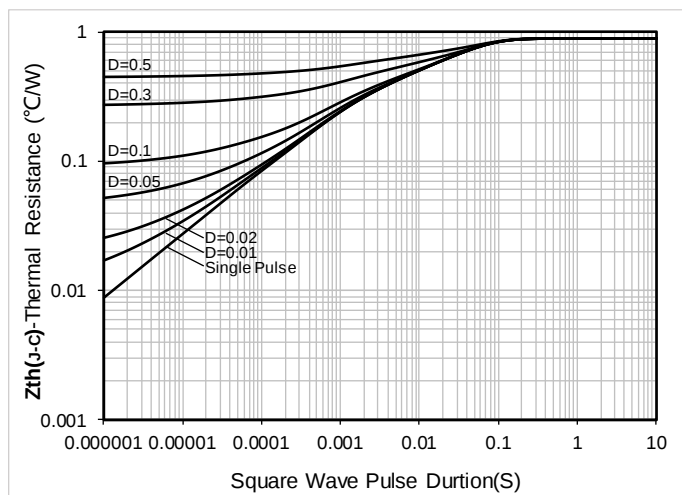


Figure 13. Maximum Transient Thermal Impedance

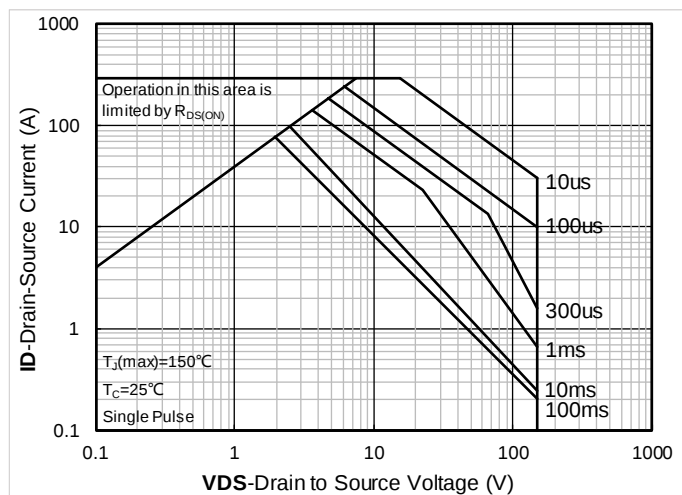
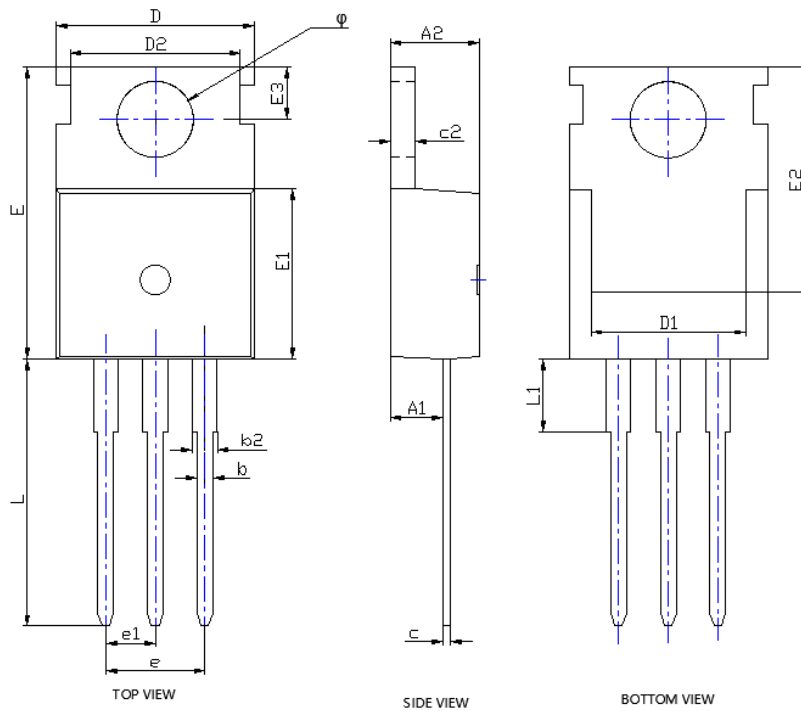


Figure 14. Safe Operation Area



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■ TO-220AB-C Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.091	0.098	2.300	2.500
A2	0.173	0.181	4.400	4.600
b	0.028	0.035	0.700	0.900
b2	0.049	0.056	1.250	1.420
c	0.018	0.022	0.450	0.550
c2	0.049	0.053	1.250	1.350
D	0.382	0.402	9.700	10.200
D1	0.295	0.331	7.500	8.400
D2	0.335	0.350	8.500	8.900
E	0.602	0.634	15.300	16.100
E1	0.358	0.366	9.100	9.300
E2	0.497	0.525	12.630	13.330
E3	0.108BSC		2.750BSC	
e	0.200BSC		5.080BSC	
e1	0.100BSC		2.540BSC	
L	0.512	0.531	13.000	13.500
L1	---	0.138	---	3.500
ϕ	0.140	0.148	3.550	3.750

NOTE:

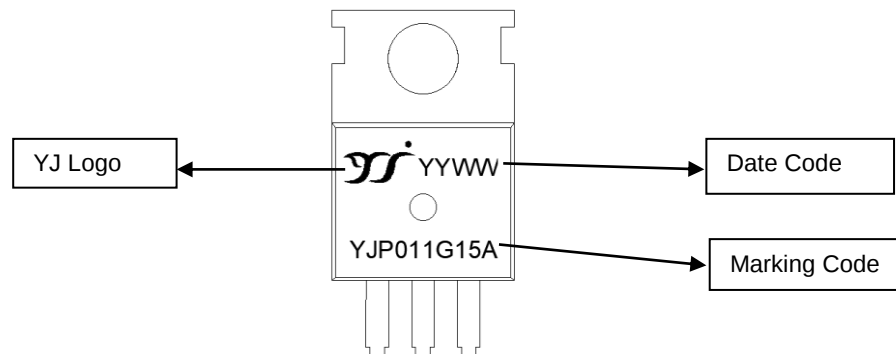
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.

2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.



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■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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