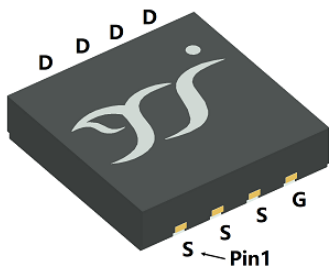
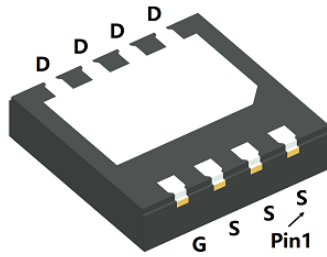




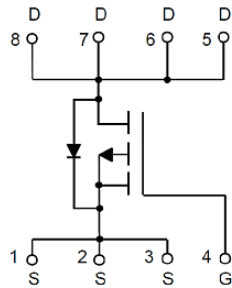
P-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View



DFN3333-8L-WF

Product Summary

• V_{DS}	-100V
• I_D	-15A
• $R_{DS(ON)}$ (at $V_{GS}=-10V$)	<120m Ω
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	
• ESD Level(HBM)	H1C

General Description

- Package with side-wettable flanks
- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power management
- Portable equipment

■ Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	-100	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^{\circ}\text{C}$, $V_{GS}= -10\text{V}$	I_D	-2.8	A
		$T_A=100^{\circ}\text{C}$, $V_{GS}= -10\text{V}$		-2	
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^{\circ}\text{C}$, $V_{GS}= -10\text{V}$		-15	
		$T_C =100^{\circ}\text{C}$, $V_{GS}= -10\text{V}$		-10.6	
Pulsed Drain Current	$T_C=25^{\circ}\text{C}$, $t_p=100\mu\text{s}$		I_{DM}	-45	A
Avalanche energy	$V_G=-10\text{V}$, $R_G=25\Omega$, $L=1\text{mH}$, $I_{AS}=-12.9\text{A}$		EAS	83.2	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^{\circ}\text{C}$	P_D	2	W
		$T_A=100^{\circ}\text{C}$		1	
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^{\circ}\text{C}$		56	
		$T_C =100^{\circ}\text{C}$		28	
Junction and Storage Temperature Range			T_J, T_{STG}	-55~+175	°C

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	60	75	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.2	2.65	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ120GP10HHQ	F1	120GP10H	5000	10000	100000	13" reel



YJQ120GP10HHQ

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V	-	-	-1	μA
		V _{DS} =-100V, V _{GS} =0V, T _J =125°C	-	-	-100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-2.0	-2.7	-3.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-15A	-	84	120	mΩ
Diode Forward Voltage	V _{SD}	I _S =-15A, V _{GS} =0V	-	-	-1.2	V
Gate resistance	R _G	f=1MHz	-	12	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	-15	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V, f=1MHz	-	900	-	pF
Output Capacitance	C _{oss}		-	110	-	
Reverse Transfer Capacitance	C _{rss}		-	6.3	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-50V, I _D =-15A	-	15.5	-	nC
Gate-Source Charge	Q _{gs}		-	2.6	-	
Gate-Drain Charge	Q _{gd}		-	2.2	-	
Reverse Recovery Charge	Q _{rr}	I _F =-15A, di/dt=100A/us	-	112	-	nC
Reverse Recovery Time	t _{rr}		-	47	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-50V, I _D =-15A R _{GEN} =3Ω	-	8	-	ns
Turn-on Rise Time	t _r		-	58	-	
Turn-off Delay Time	t _{D(off)}		-	27	-	
Turn-off fall Time	t _f		-	13.5	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).



YJQ120GP10HHQ

■ Typical Electrical and Thermal Characteristics Diagrams

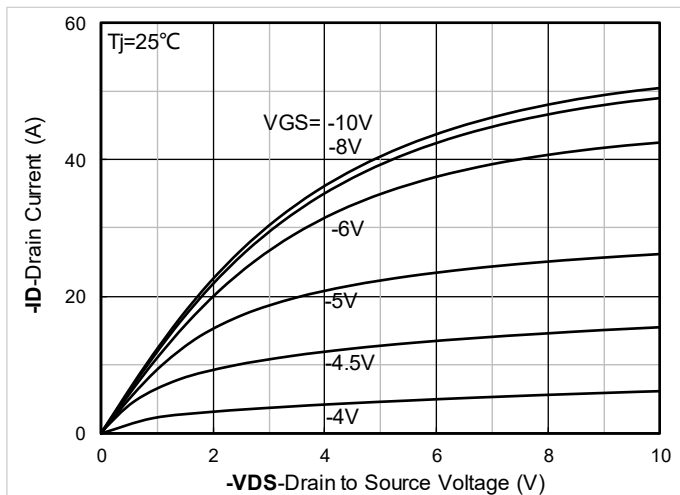


Figure 1. Output Characteristics

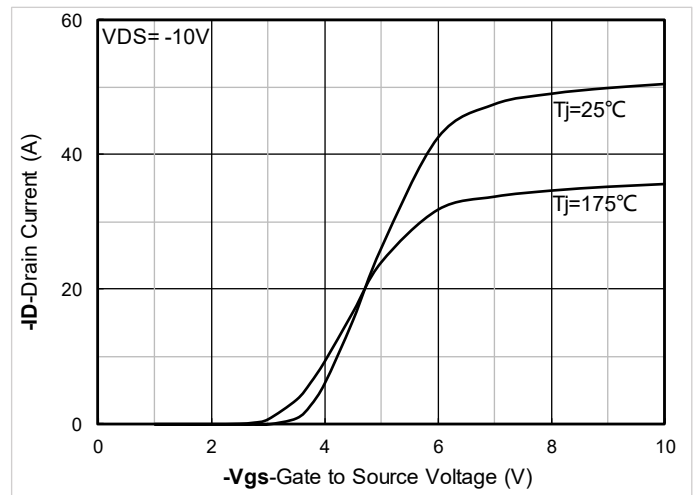


Figure 2. Transfer Characteristics

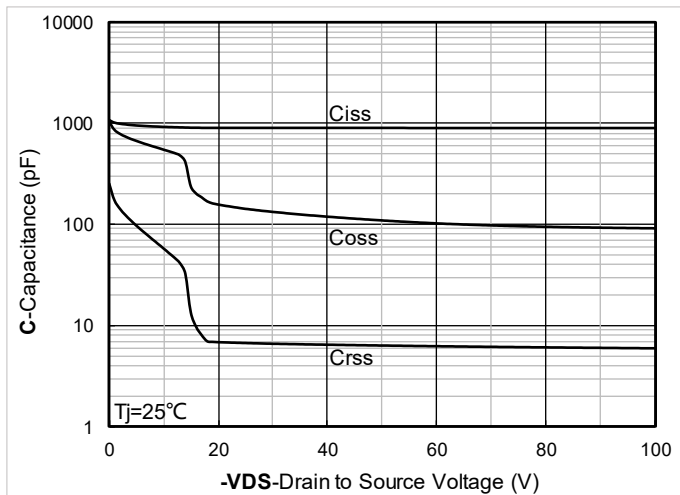


Figure 3. Capacitance Characteristics

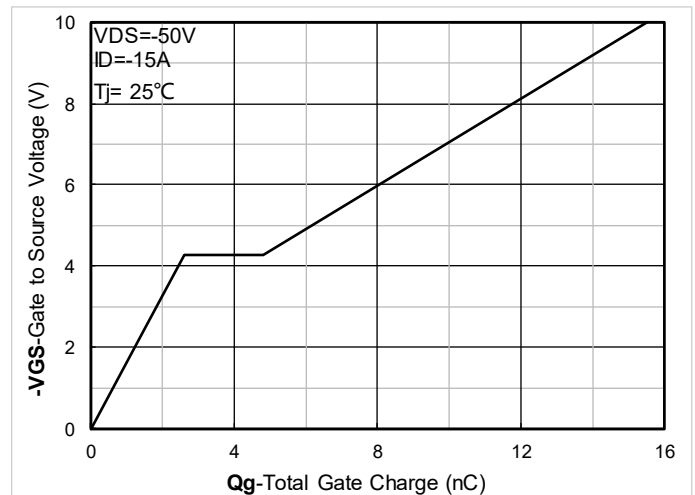


Figure 4. Gate Charge

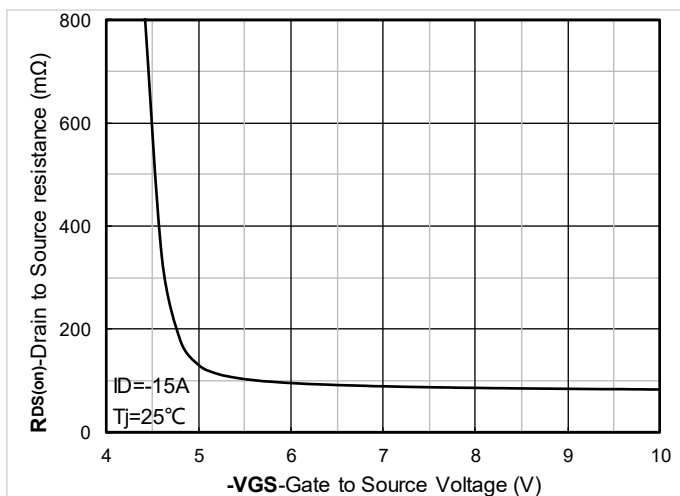


Figure 5. On-Resistance vs Gate to Source Voltage

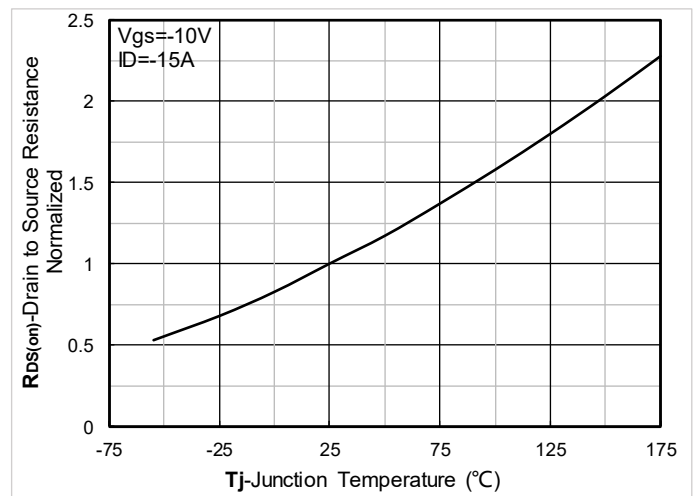


Figure 6. Normalized On-Resistance

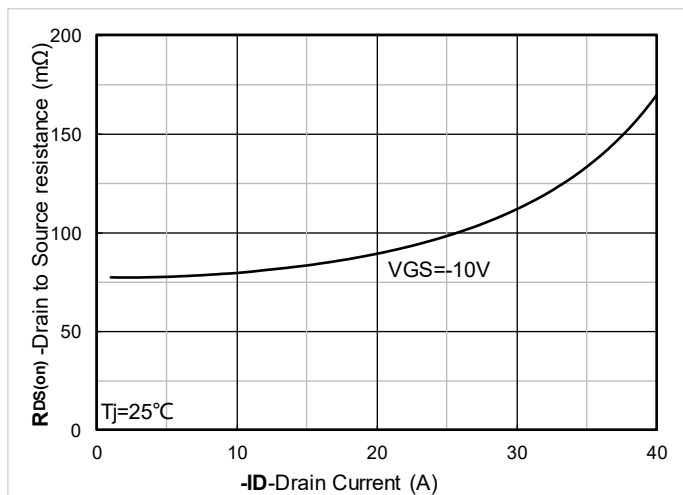


Figure 7. $R_{DS(on)}$ VS Drain Current

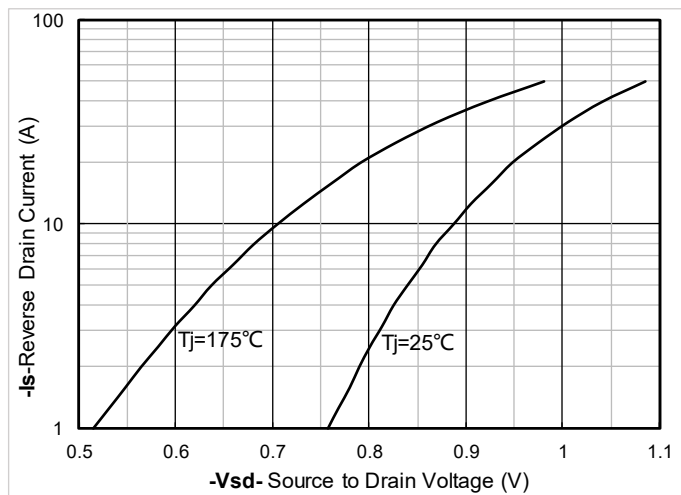


Figure 8. Forward characteristics of reverse diode

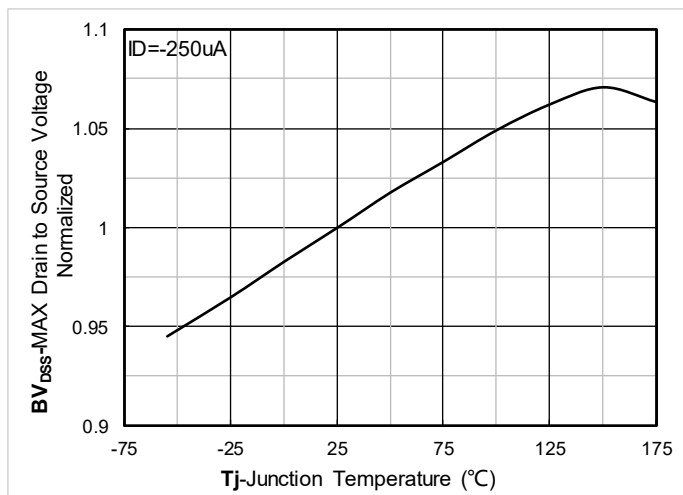


Figure 9. Normalized breakdown voltage

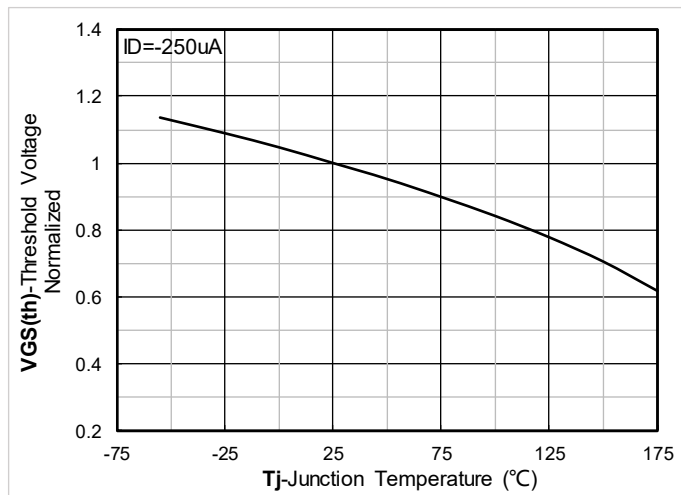


Figure 10. Normalized Threshold voltage

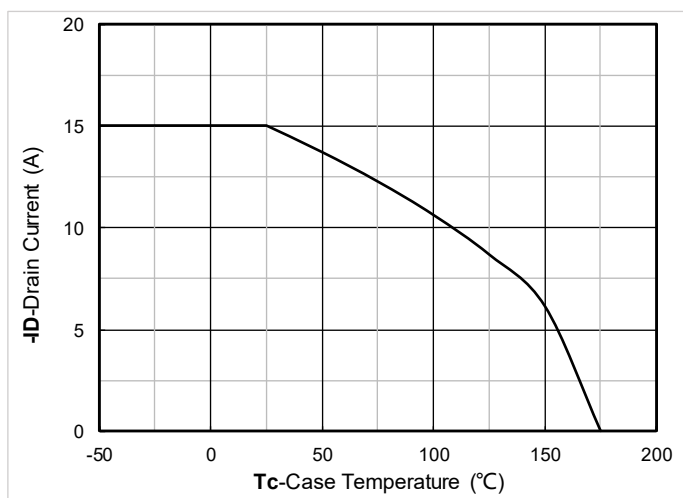


Figure 11. Current dissipation

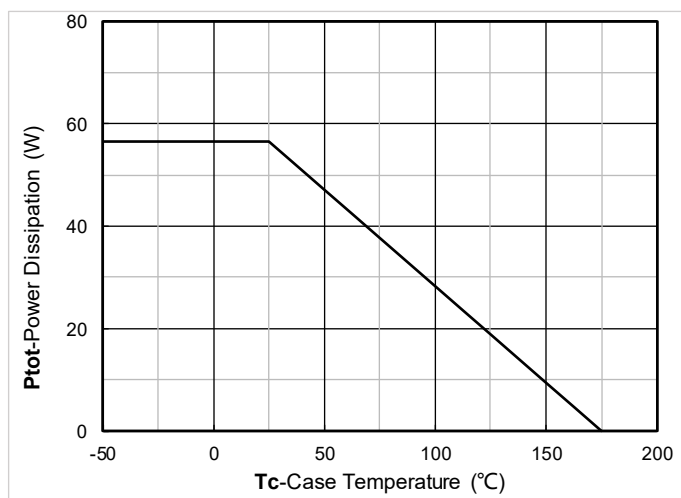


Figure 12. Power dissipation

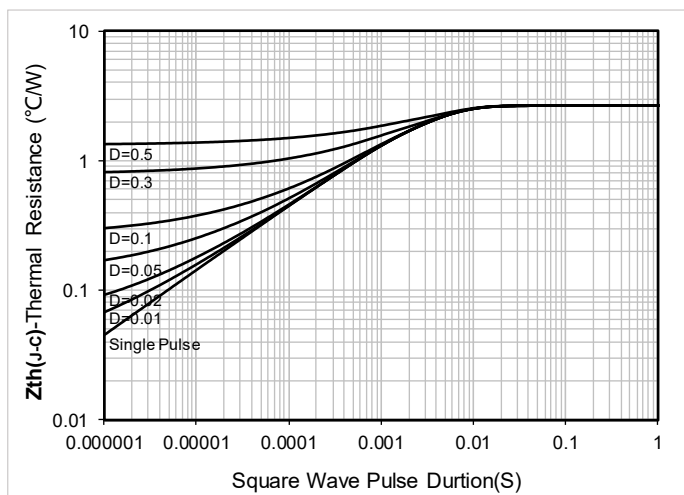


Figure 13. Maximum Transient Thermal Impedance

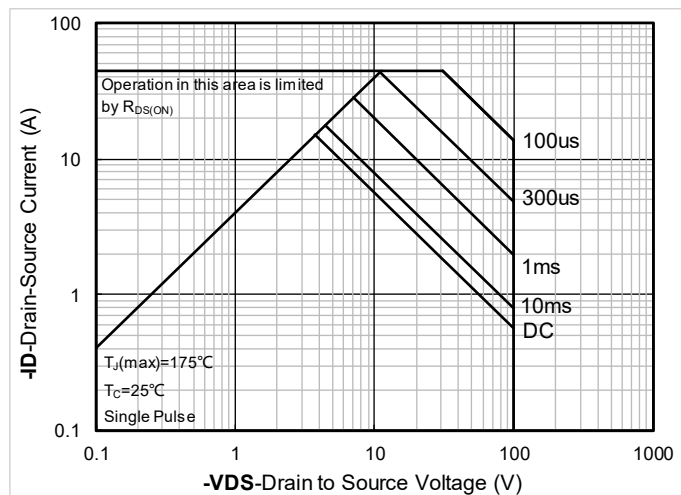
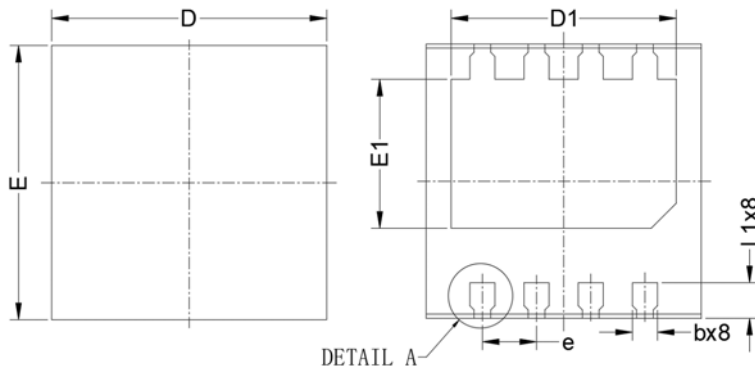


Figure 14. Safe Operation Area



YJQ120GP10HHQ

■ DFN3333-8L-WF Package information



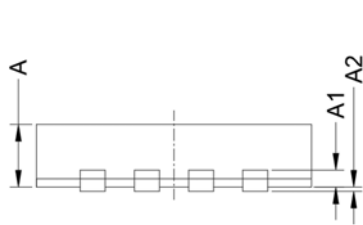
Top View
正面视图

Bottom View
背面视图

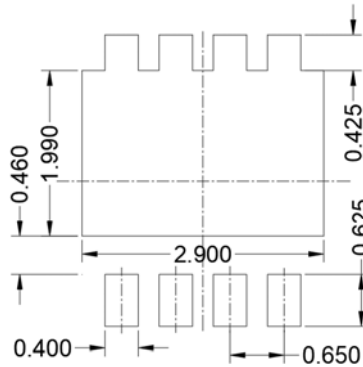
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D		3.30 BSC	
E		3.30 BSC	
A	0.70	0.75	0.80
A1		0.203 BSC	
A2			0.10
D1	2.60	2.70	2.80
E1	1.69	1.79	1.89
L1	0.325	0.425	0.525
b	0.20	0.30	0.40
e		0.65 BSC	

Note:

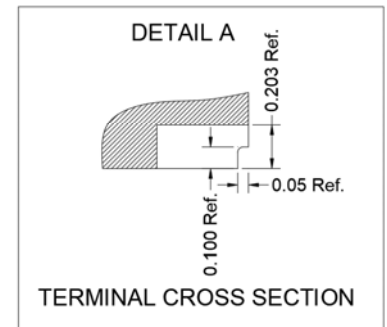
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.



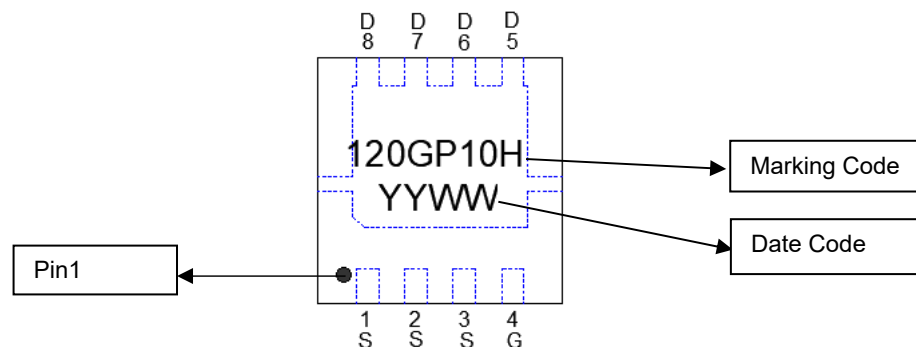
Side View
侧面视图



Suggested Solder Pad Layout
Top View



■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. 120GP10H is marking code, YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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