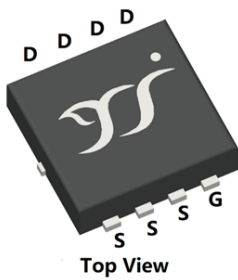
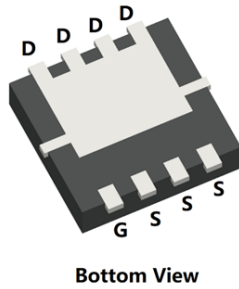




N-Channel Enhancement Mode Field Effect Transistor

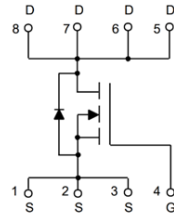


Top View



Bottom View

PDFN3333-8L



Product Summary

- V_{DS} 30V
- I_D 109A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<3m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Intrinsic fast-recovery body diode
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- 30V HS+LS PC Application

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	30	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} =10V	I _D	-	19.9	A
		T _A =100°C,V _{GS} =10V		-	12.6	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} =10V,Chip limitation		-	109	
		T _C =100°C,V _{GS} =10V		-	68.9	
Pulsed Drain Current	T _C =25°C,t _p ≤10μs		I _{DM}	-	436	
Maximum Body-Diode Continuous Current	T _C =25°C		I _S		47	
Avalanche Energy (non-repetitive)	T _J =25°C,V _G =10V,R _G =25Ω,L=0.5mH,I _{AS} =19.6A		EAS	-	96	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	1.89	W
		T _A =100°C		-	0.75	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	56.8	
		T _C =100°C		-	22.7	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	150	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	66	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	2.2	



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■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A, T_j=25^\circ C$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V, T_j=25^\circ C$	-	-	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_j=125^\circ C$	-	-	100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V, T_j=25^\circ C$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A, T_j=25^\circ C$	1.2	1.9	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A, T_j=25^\circ C$	-	2.4	3	m Ω
Diode Forward Voltage	V_{SD}	$I_S=50A, V_{GS}=0V, T_j=25^\circ C$	-	0.87	1.2	V
Gate Resistance	R_G	$f=1MHz, T_j=25^\circ C$	-	1.2	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V, f=1MHz, T_j=25^\circ C$	-	1424	-	pF
Output Capacitance	C_{oss}		-	1208	-	
Reverse Transfer Capacitance	C_{rss}		-	47	-	
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=15V, I_D=50A, T_j=25^\circ C$	-	25.7	-	nC
Gate-Source Charge	Q_{gs}		-	4.7	-	
Gate-Drain Charge	Q_{gd}		-	7.6	-	
Reverse Recovery Charge	Q_{rr}	$I_F=50A, di/dt=100A/\mu s, V_{GS}=0V, V_R=15V, T_j=25^\circ C$	-	12.7	-	nC
Reverse Recovery Time	t_{rr}		-	25.5	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, I_D=50A, R_{GEN}=3\Omega, T_j=25^\circ C$	-	10.8	-	ns
Turn-on Rise Time	t_r		-	11.3	-	
Turn-off Delay Time	$t_{D(off)}$		-	22.9	-	
Turn-off Fall Time	t_f		-	7.4	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

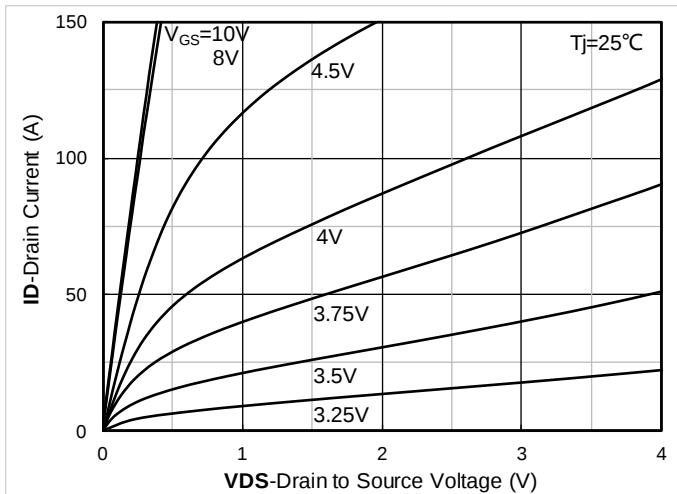


Figure 1. Output Characteristics; typical values

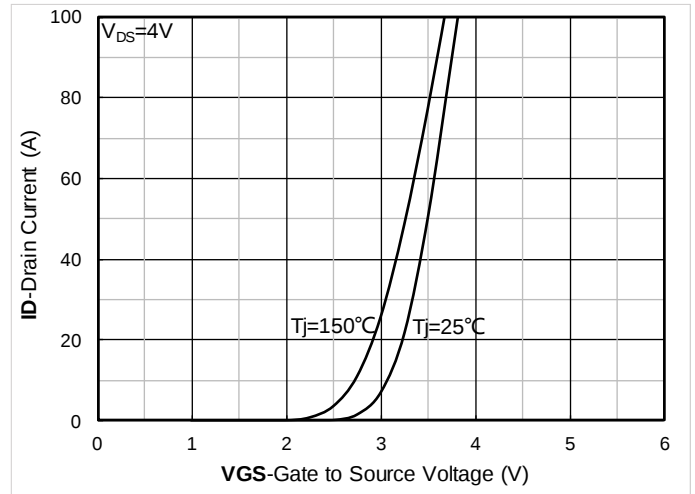


Figure 2. Transfer Characteristics; typical values

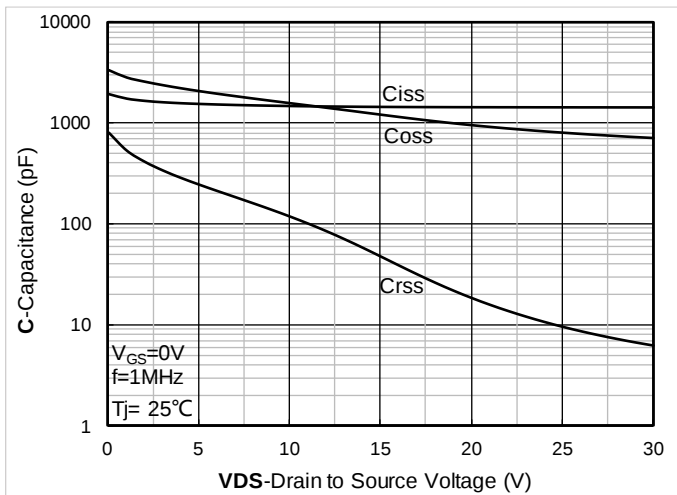


Figure 3. Capacitance Characteristics; typical values

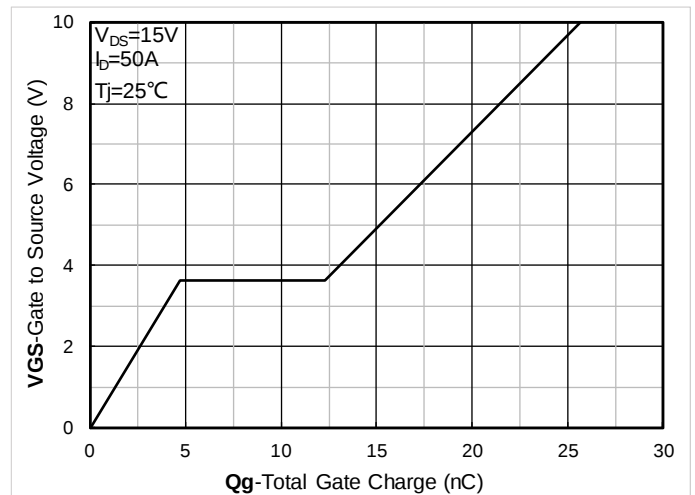


Figure 4. Gate Charge; typical values

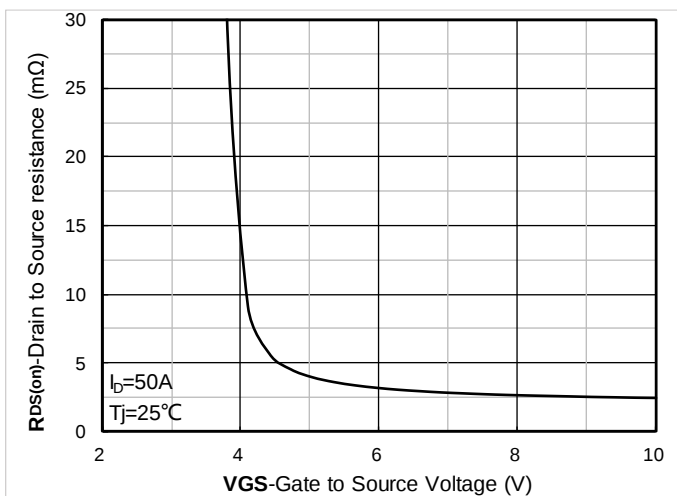


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

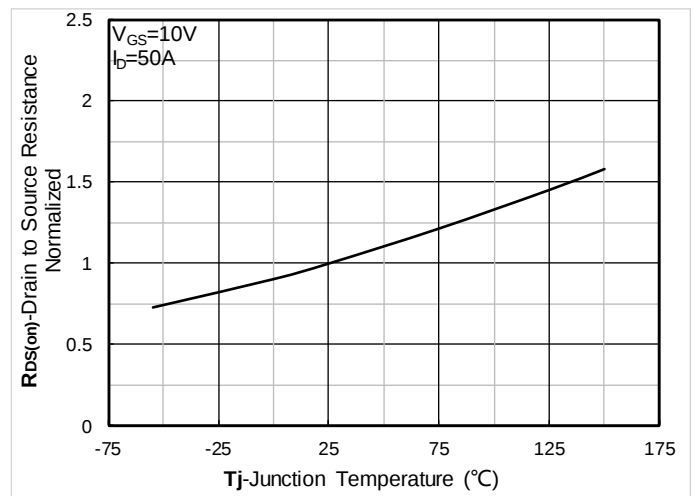


Figure 6. Normalized On-Resistance



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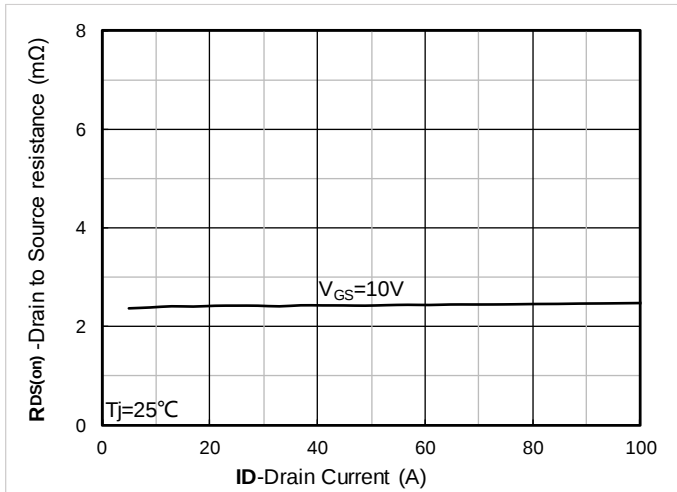


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

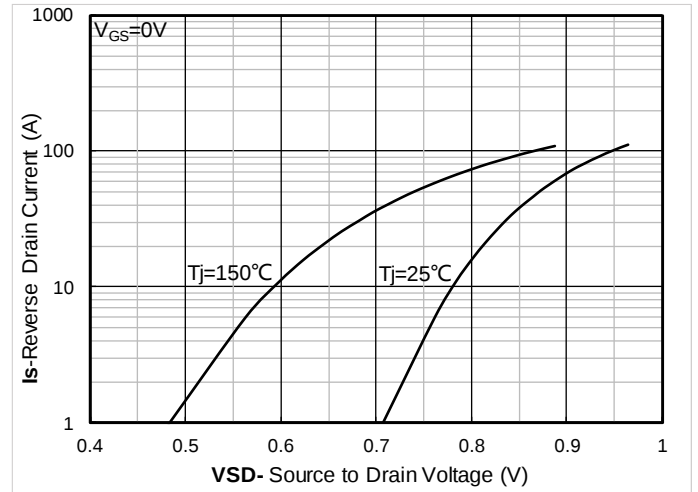


Figure 8. Forward characteristics of reverse diode; typical values

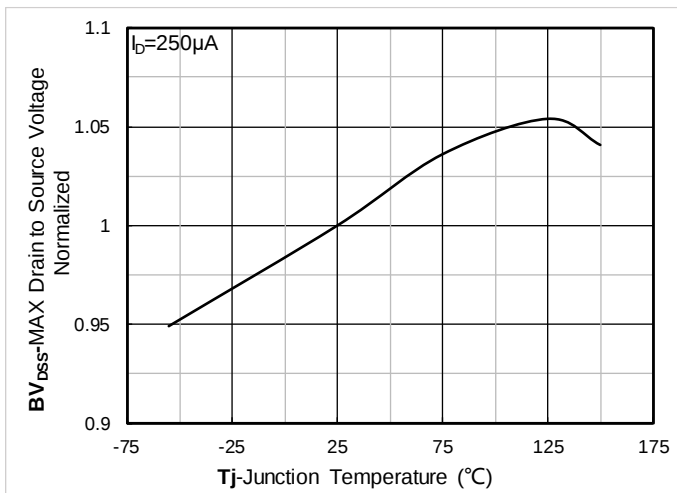


Figure 9. Normalized breakdown voltage

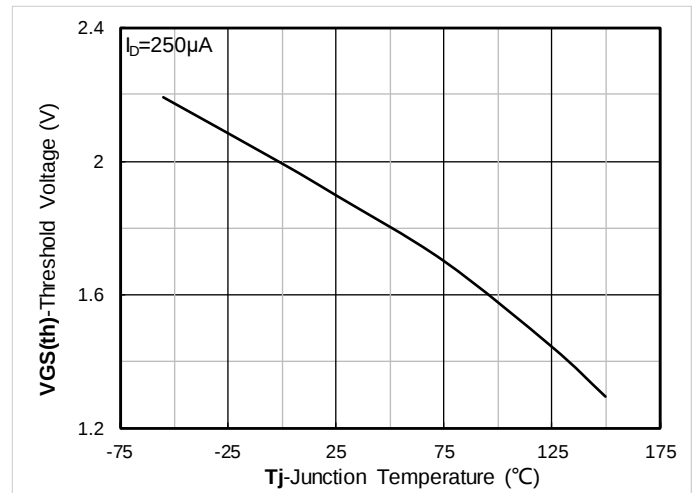


Figure 10. Gate Threshold voltage; typical values

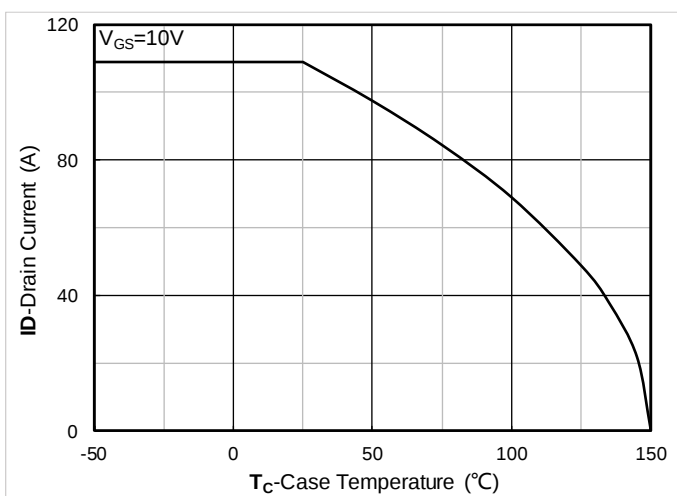


Figure 11. Current dissipation

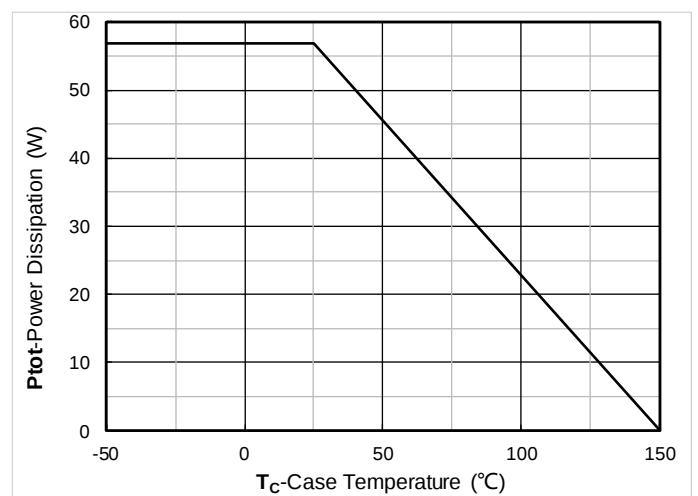


Figure 12. Power dissipation

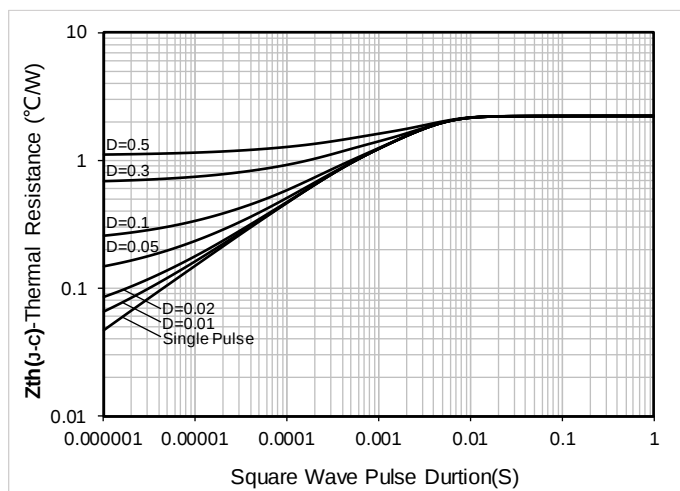


Figure 13. Maximum Transient Thermal Impedance

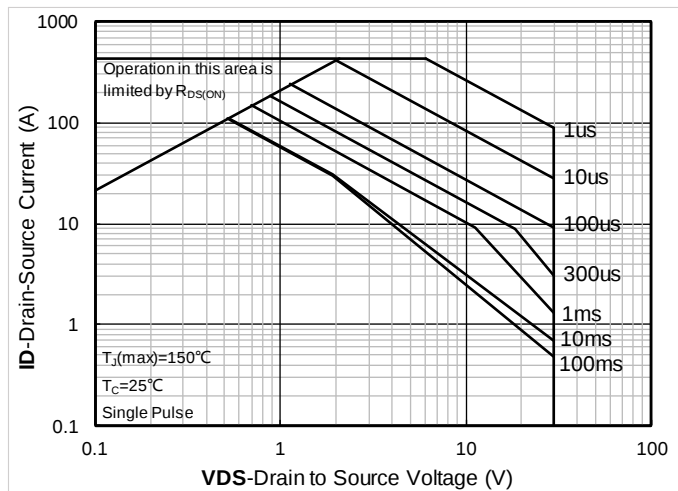
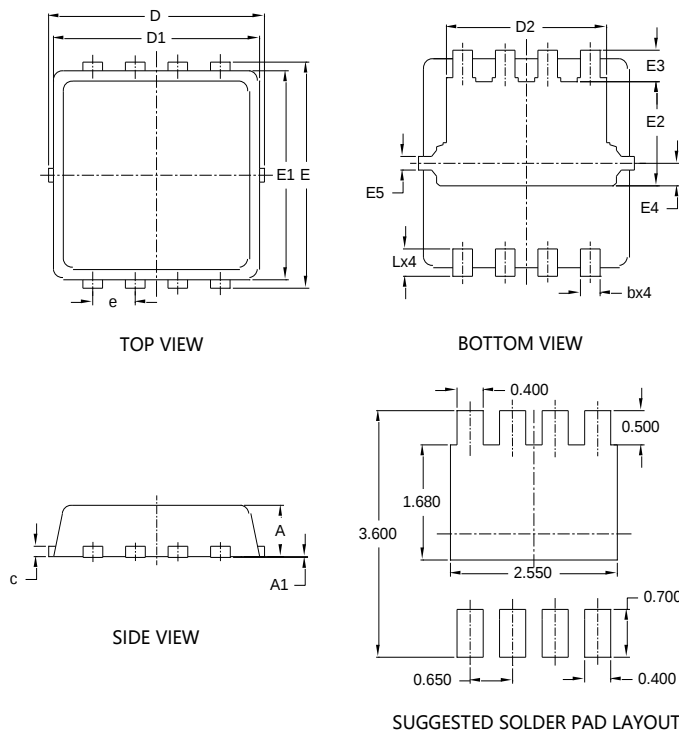


Figure 14. Safe Operation Area



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■ PDFN3333-8L-B-0.75mm Package information



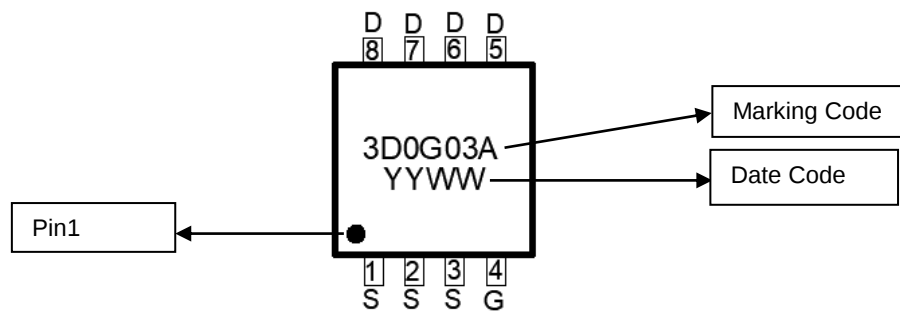
SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.028	0.033	0.700	0.850
A1	0.000	0.002	0.000	0.050
b	0.008	0.016	0.200	0.400
c	0.004	0.010	0.100	0.250
D	0.124	0.136	3.150	3.450
D1	0.118	0.130	3.000	3.300
D2	0.089	0.104	2.250	2.650
E	0.124	0.136	3.150	3.450
E1	0.114	0.126	2.900	3.200
E2	0.052	0.068	1.320	1.720
E3	0.011	0.026	0.280	0.650
E4	0.013 REF		0.330 REF	
E5	0.008 REF		0.200 REF	
e	0.026 BSC		0.650 BSC	
L	0.012	0.020	0.300	0.500

NOTE:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

UNIT: mm



■ Marking Information



- Note:
1. All marking is at middle of the product body
 2. All marking is in laser printing
 3. YYWW is date code, "YY" is year, "WW" is week
 4. Body color: Black



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