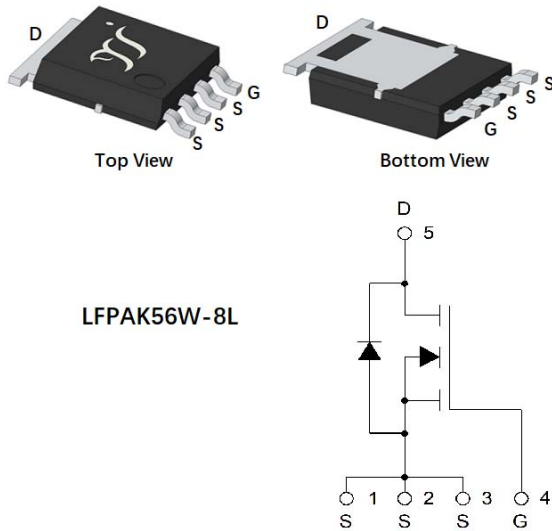


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

• V_{DS}	100V
• I_D	26A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<32m Ω
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<46m Ω
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	
• ESD Level(HBM)	H1A

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Automotive motor control

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-Source Voltage			V _{DS}	-	100	V
Gate-Source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} =10V	I _D	-	5.8	A
		T _A =100°C,V _{GS} =10V		-	4.1	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} =10V,Chip limitation		-	26	
		T _C =100°C,V _{GS} =10V		-	18.3	
Pulsed Drain Current	T _C =25°C,t _p ≤10μs		I _{DM}	-	104	
Maximum Body-Diode Continuous Current	T _C =25°C		I _S	-	26	
Avalanche Energy (non-repetitive)	T _J =25°C,V _G =10V,R _G =25Ω,L=0.5mH,I _{AS} =11A		EAS	-	30.2	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	2.54	W
		T _A =100°C		-	1.27	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	50	
		T _C =100°C		-	25	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	175	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	59	$^{\circ}\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	3	



YJYA032G10AQ

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=1mA, T_j=25^{\circ}C$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V, T_j=25^{\circ}C$	-	-	1	μA
		$V_{DS}=80V, V_{GS}=0V, T_j=125^{\circ}C$	-	-	100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V, T_j=25^{\circ}C$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A, T_j=25^{\circ}C$	1	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A, T_j=25^{\circ}C$	-	24	32	m Ω
		$V_{GS}=4.5V, I_D=10A, T_j=25^{\circ}C$	-	31	46	m Ω
Diode Forward Voltage	V_{SD}	$I_S=20A, V_{GS}=0V, T_j=25^{\circ}C$	-	0.94	1.2	V
Gate Resistance	R_G	$f=1MHz, T_j=25^{\circ}C$	-	1	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V, f=1MHz, T_j=25^{\circ}C$	-	514	-	pF
Output Capacitance	C_{oss}		-	117	-	
Reverse Transfer Capacitance	C_{rss}		-	2.5	-	
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=50V, I_D=20A, T_j=25^{\circ}C$	-	11.6	-	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	
Gate-Drain Charge	Q_{gd}		-	3.8	-	
Reverse Recovery Charge	Q_{rr}	$I_F=20A, di/dt=100A/\mu s, V_{GS}=0V, V_R=50V, T_j=25^{\circ}C$	-	30	-	nC
Reverse Recovery Time	t_{rr}		-	32	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=50V, I_D=20A, R_{GEN}=3\Omega, T_j=25^{\circ}C$	-	6.4	-	ns
Turn-on Rise Time	t_r		-	3.7	-	
Turn-off Delay Time	$t_{D(off)}$		-	15.4	-	
Turn-off Fall Time	t_f		-	4.1	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^{\circ}C$. The maximum allowed junction temperature of 175 $^{\circ}C$. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

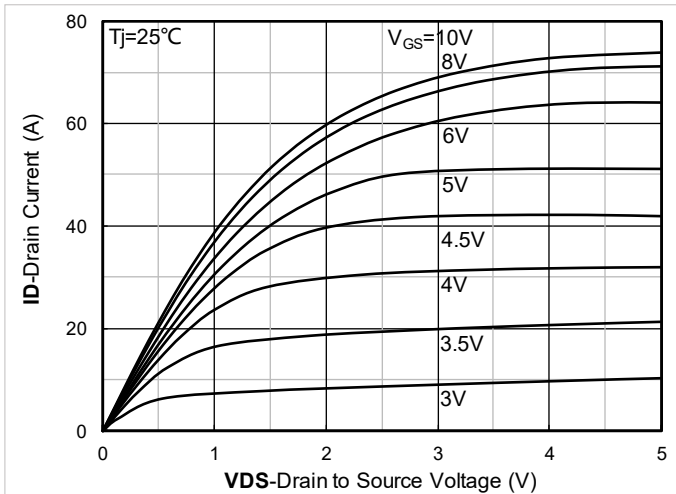


Figure 1. Output Characteristics; typical values

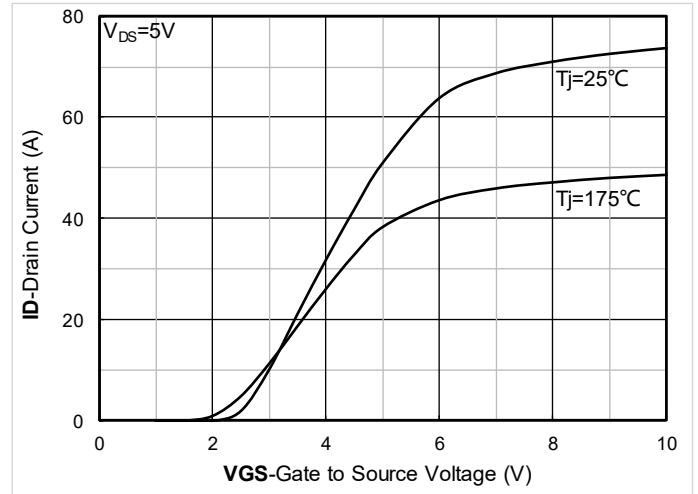


Figure 2. Transfer Characteristics; typical values

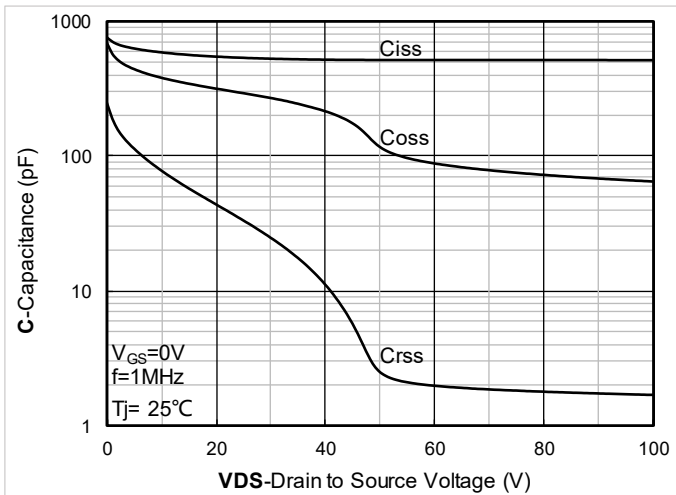


Figure 3. Capacitance Characteristics; typical values

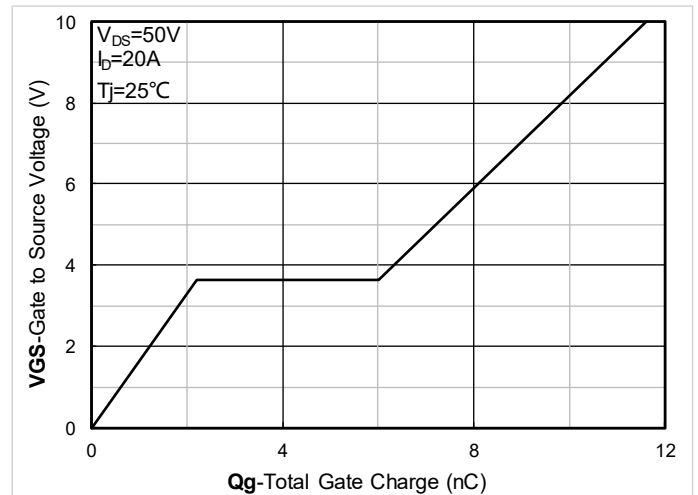


Figure 4. Gate Charge; typical values

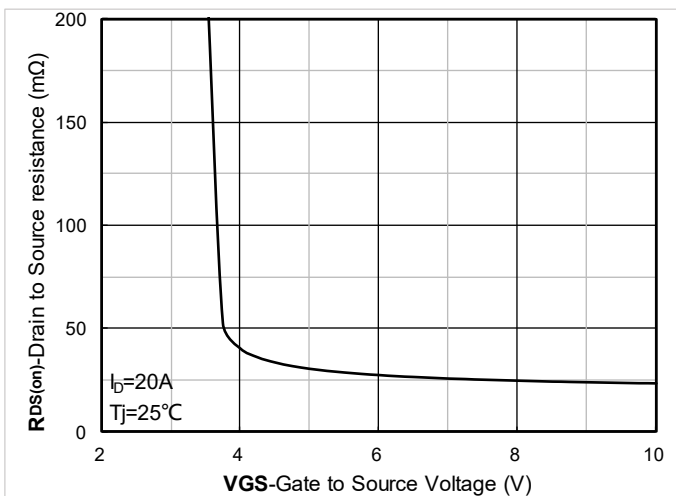


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

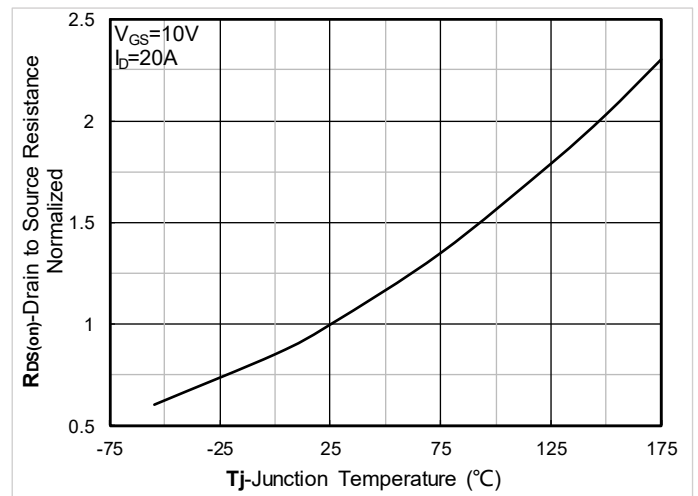


Figure 6. Normalized On-Resistance

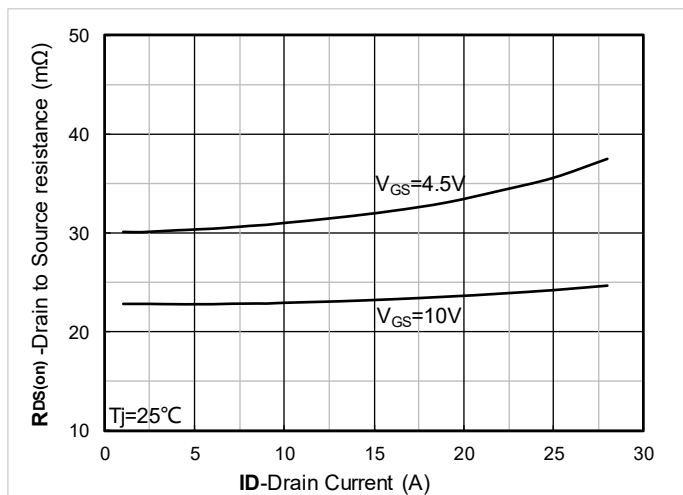


Figure 7. RDS(on) vs. Drain Current; typical values

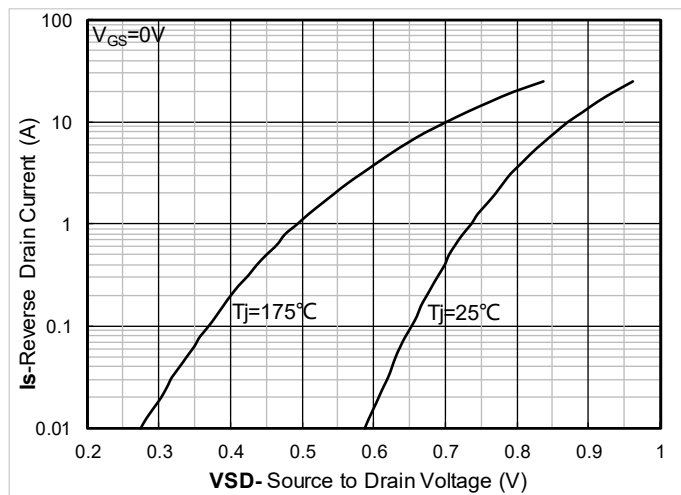


Figure 8. Forward characteristics of reverse diode; typical values

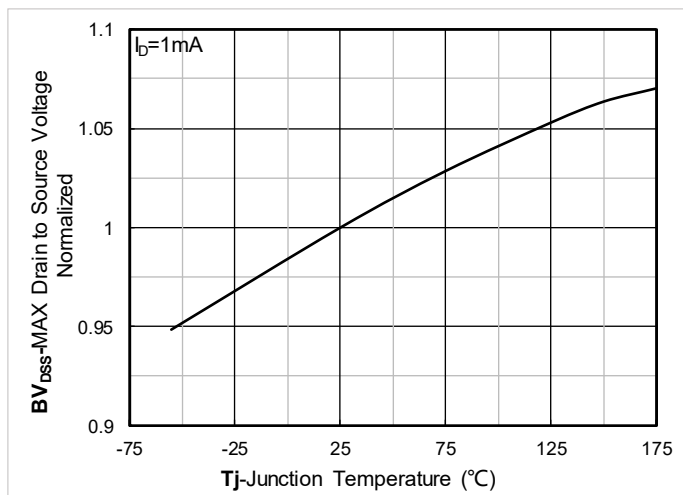


Figure 9. Normalized breakdown voltage

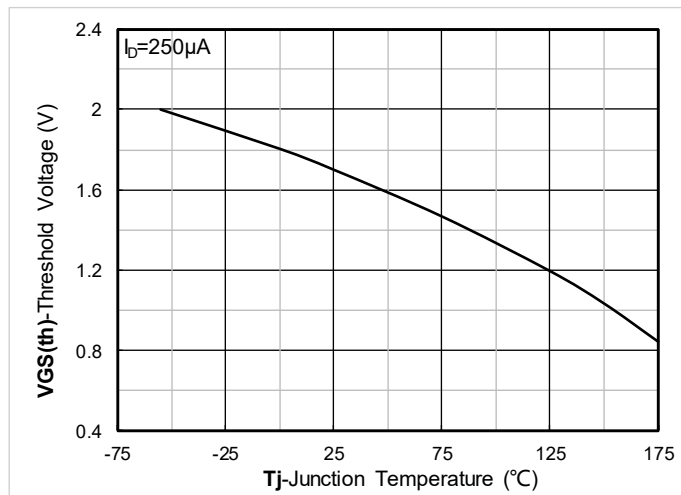


Figure 10. Gate Threshold voltage; typical values

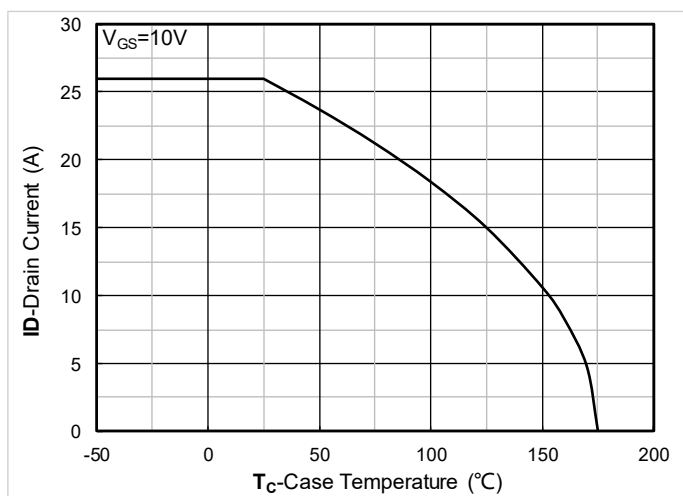


Figure 11. Current dissipation

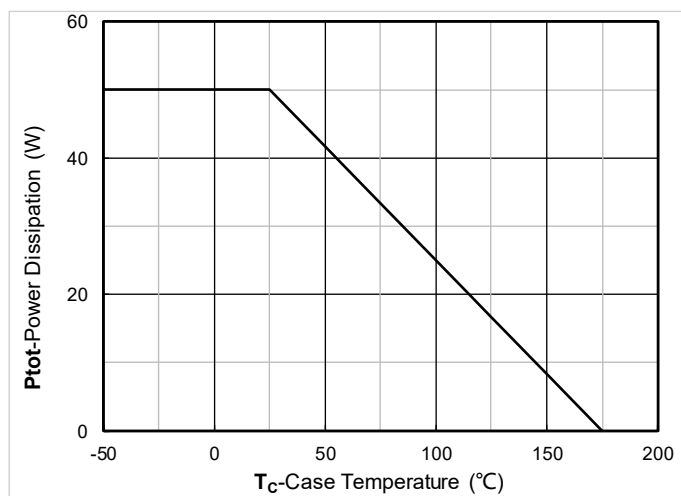


Figure 12. Power dissipation

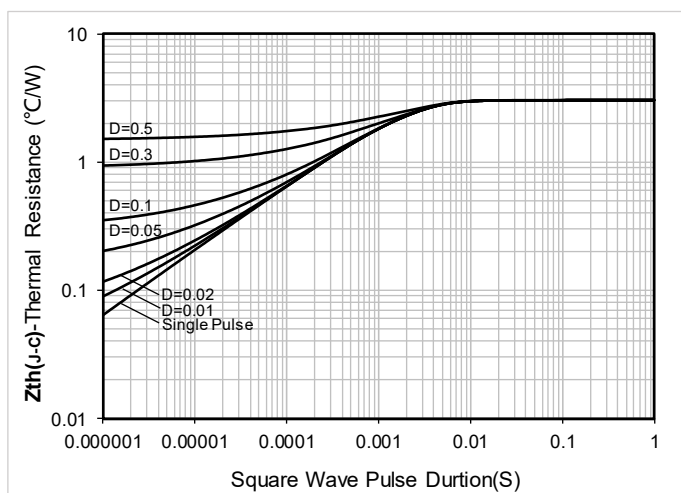


Figure 13. Maximum Transient Thermal Impedance

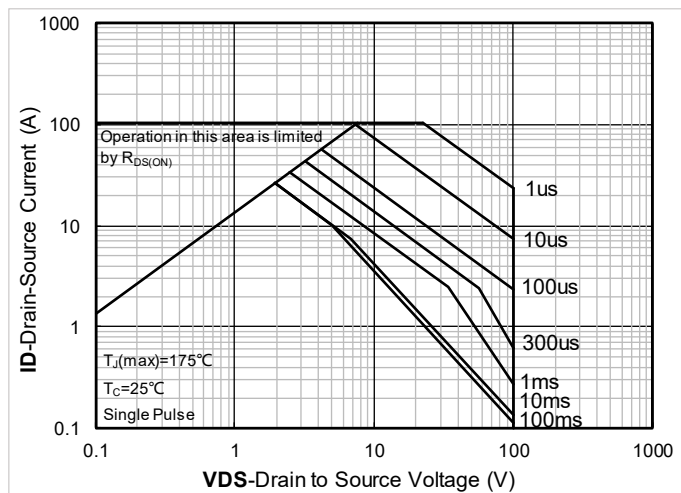
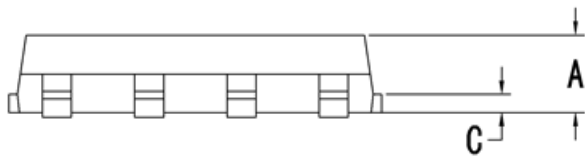
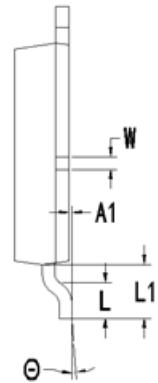
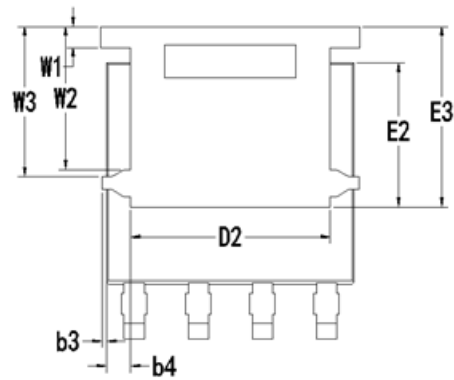
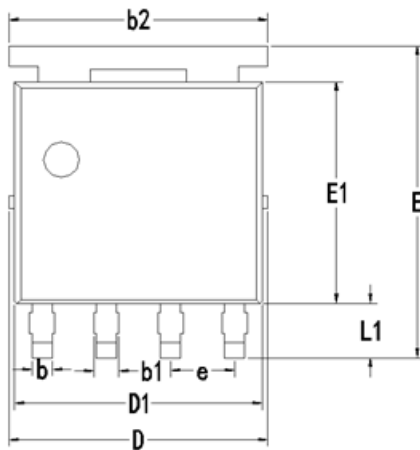


Figure 14. Safe Operation Area



YJYA032G10AQ

■ LFPAK56W-8L-A-1.04MM Package information



Note:

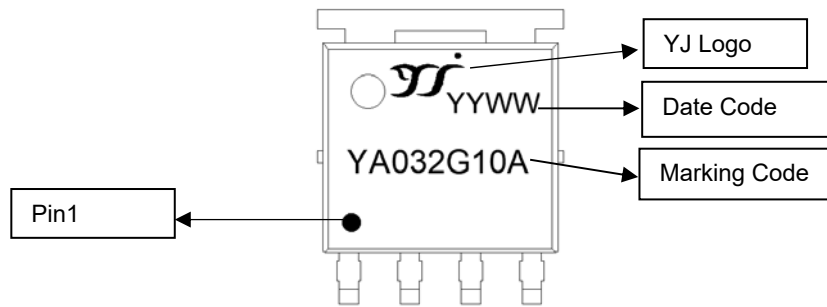
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.04	1.07
A1	0.00	0.06	0.127
b	0.33	0.41	0.48
b1	0.44	0.51	0.58
b2	4.80	4.90	5.00
b3	-	0.094	-
b4	-	0.47	-
c	0.20	0.254	0.30
D	5.00	5.10	5.25
D1	4.80	4.90	5.00
D2	3.86	3.96	4.06
E	6.05	6.15	6.25
E1	4.27	4.37	4.47
E2	2.75	2.85	2.95
E3	3.46	3.56	3.66
e	1.27		
L	0.62	0.72	0.82
L1	0.92	1.07	1.22
W	-	0.23 BSC	-
W1	-	0.41 BSC	-
W2	-	2.82 BSC	-
W3	-	2.96 BSC	-
Θ	0°		10°



YJYA032G10AQ

■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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