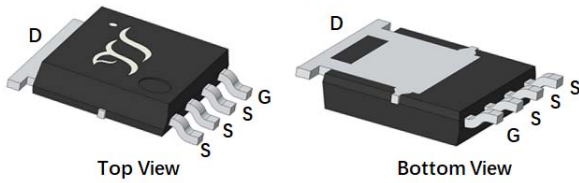
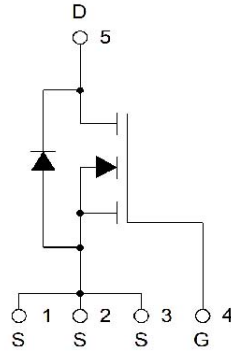


N-Channel Enhancement Mode Field Effect Transistor



LFPAK56W-8L



Product Summary

• V_{DS}	40V
• I_D	100A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	$<2.9m\Omega$
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	
• ESD Level(HBM)	H1B

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Automotive engine control
- Solenoid and motor drivers
- Powertrain management

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	40	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} =10V	I _D	-	22.5	A
		T _A =100°C,V _{GS} =10V		-	15.9	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} =10V,Chip limitation		-	100	
		T _C =100°C,V _{GS} =10V		-	70.7	
Pulsed Drain Current	T _C =25°C,t _p ≤10μs		I _{DM}	-	400	A
Maximum Body-Diode Continuous Current	T _C =25°C		I _S		83	
Avalanche Energy (non-repetitive)	T _J =25°C,V _G =10V,R _G =25Ω,L=0.5mH,I _{AS} =29A		EAS	-	210.2	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	2.67	W
		T _A =100°C		-	1.33	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	100	
		T _C =100°C		-	50	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	175	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	56	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	1.5	



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■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =1mA, T _J =25°C	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V, T _J =25°C	-	-	1	μA
		V _{DS} =40V, V _{GS} =0V, T _J =125°C	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _J =25°C	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA, T _J =25°C	2	2.8	3.6	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =50A, T _J =25°C	-	2.2	2.9	mΩ
Diode Forward Voltage	V _{SD}	I _S =50A, V _{GS} =0V, T _J =25°C	-	0.87	1.2	V
Gate Resistance	R _G	f=1MHz, T _J =25°C	-	3	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1MHz, T _J =25°C	-	2404	-	pF
Output Capacitance	C _{oss}		-	789	-	
Reverse Transfer Capacitance	C _{rss}		-	26	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =50A, T _J =25°C	-	33.4	-	nC
Gate-Source Charge	Q _{gs}		-	11.7	-	
Gate-Drain Charge	Q _{gd}		-	6.7	-	
Reverse Recovery Charge	Q _{rr}	I _F =50A, di/dt=100A/μs, V _{GS} =0V, V _R =20V, T _J =25°C	-	13	-	nC
Reverse Recovery Time	t _{rr}		-	24.5	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =20V, I _D =50A, R _{GEN} =3Ω, T _J =25°C	-	16.7	-	ns
Turn-on Rise Time	t _r		-	122.2	-	
Turn-off Delay Time	t _{D(off)}		-	27	-	
Turn-off Fall Time	t _f		-	11.3	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^{\circ}C$. The maximum allowed junction temperature of 175 $^{\circ}C$. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

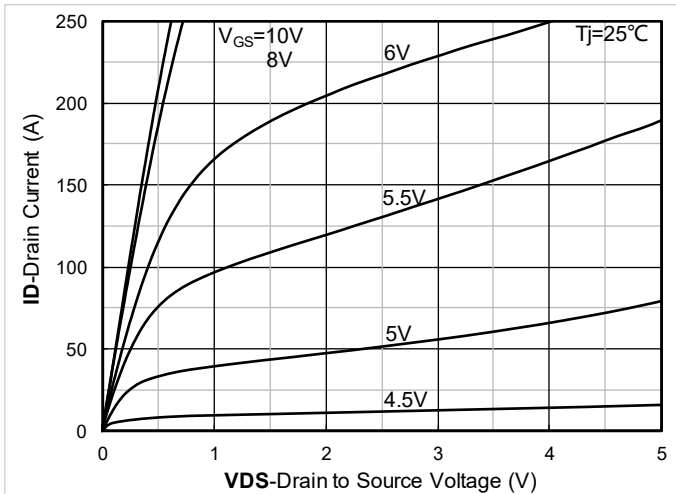


Figure 1. Output Characteristics; typical values

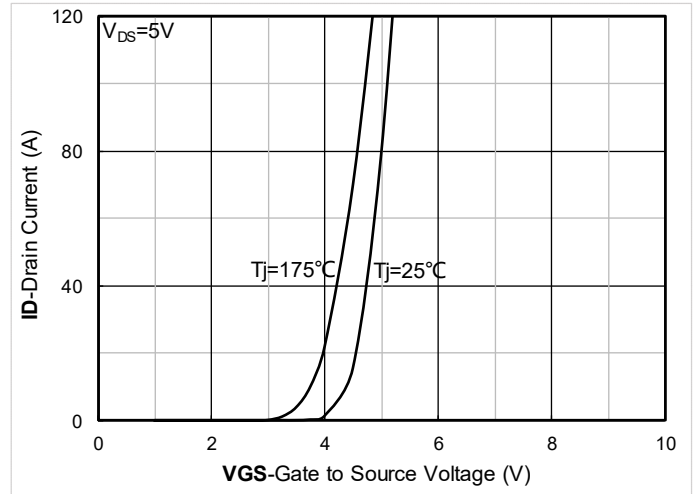


Figure 2. Transfer Characteristics; typical values

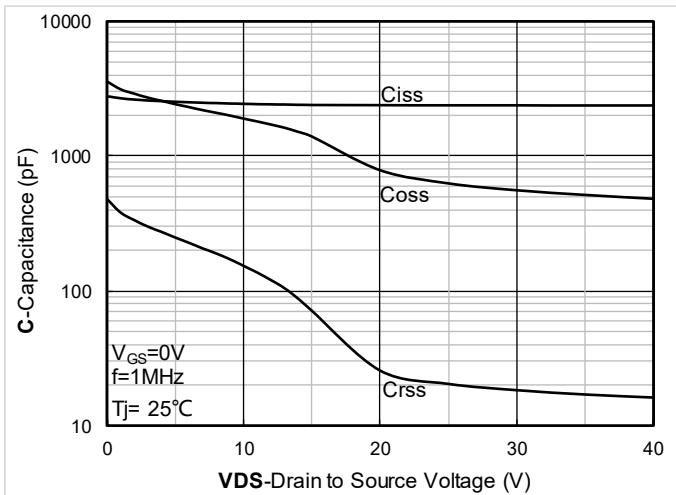


Figure 3. Capacitance Characteristics; typical values

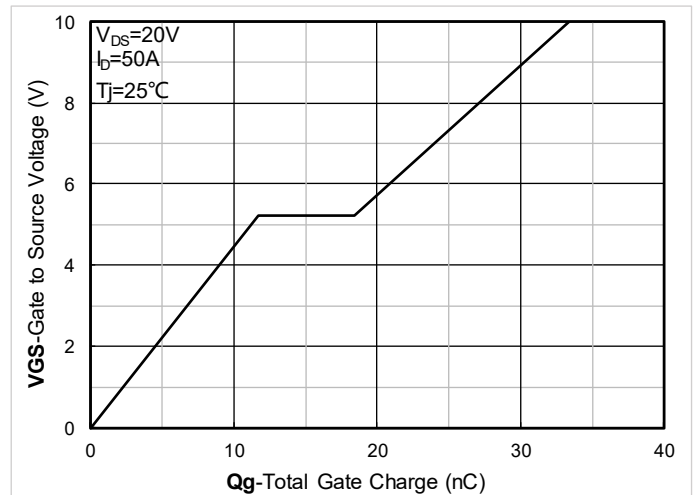


Figure 4. Gate Charge; typical values

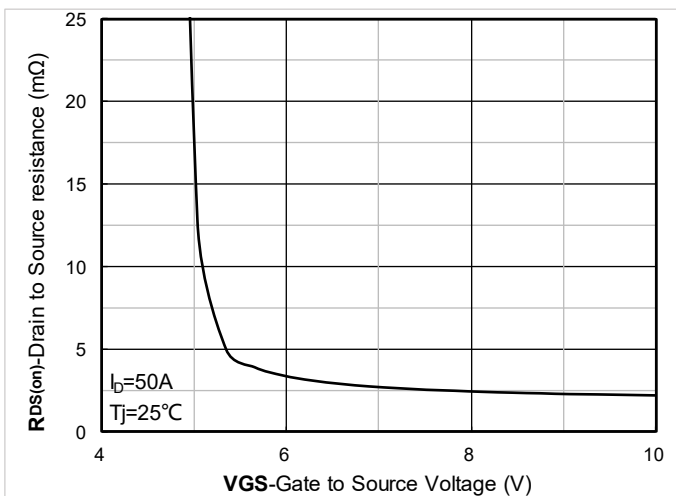


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

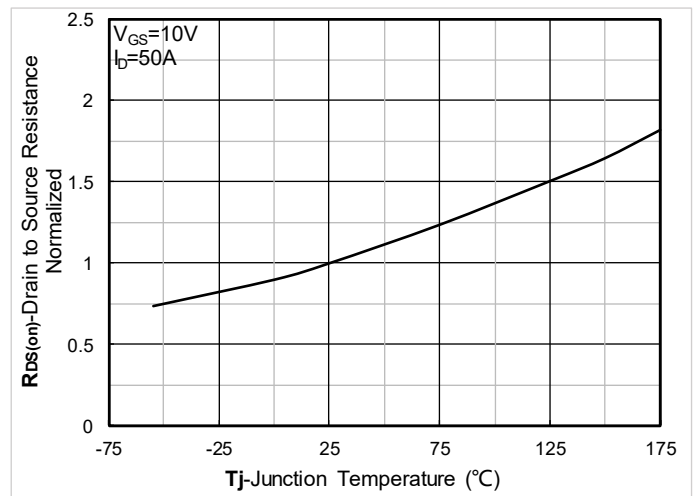


Figure 6. Normalized On-Resistance

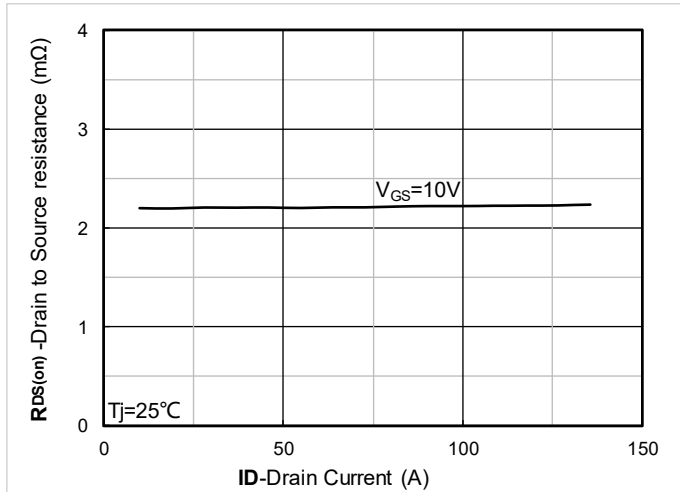


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

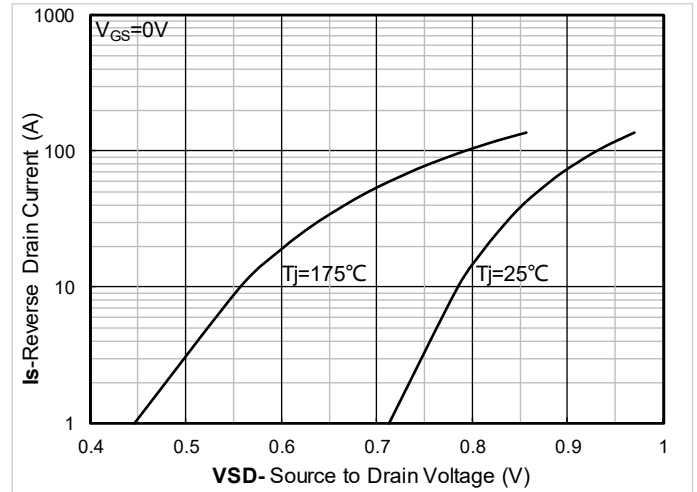


Figure 8. Forward characteristics of reverse diode; typical values

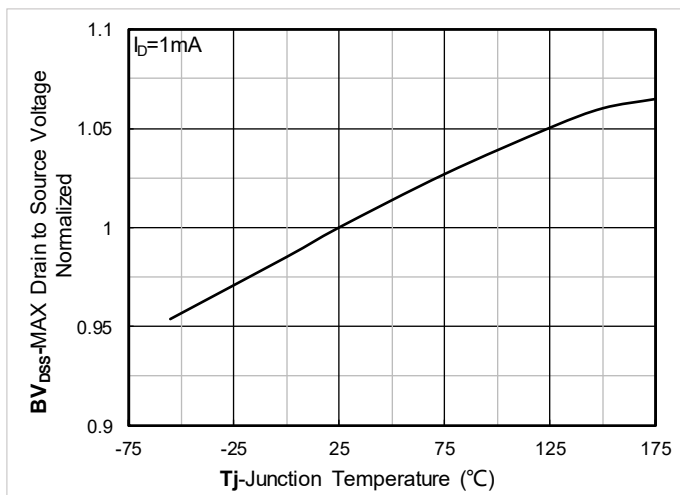


Figure 9. Normalized breakdown voltage

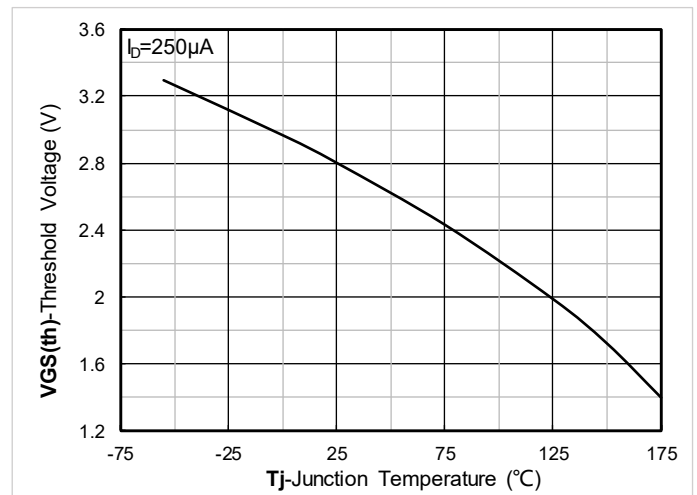


Figure 10. Gate Threshold voltage; typical values

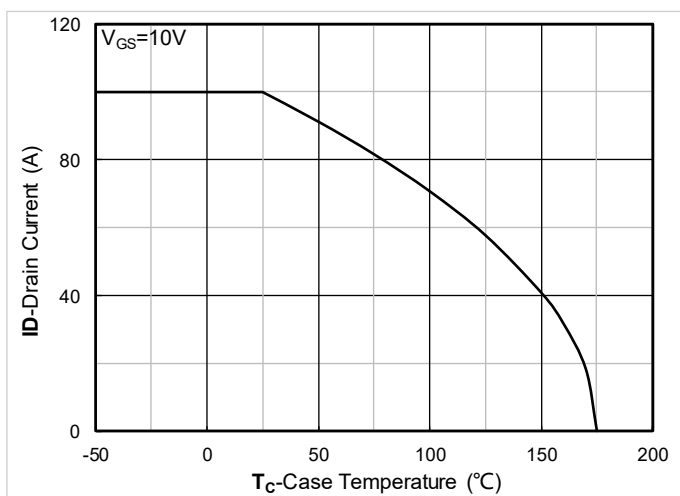


Figure 11. Current dissipation

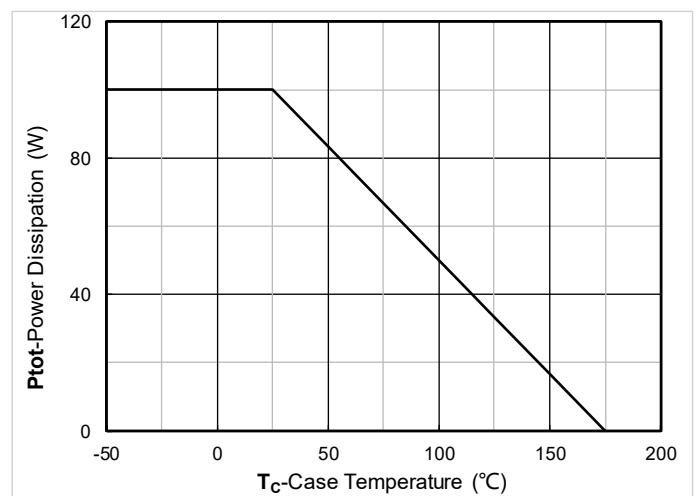


Figure 12. Power dissipation

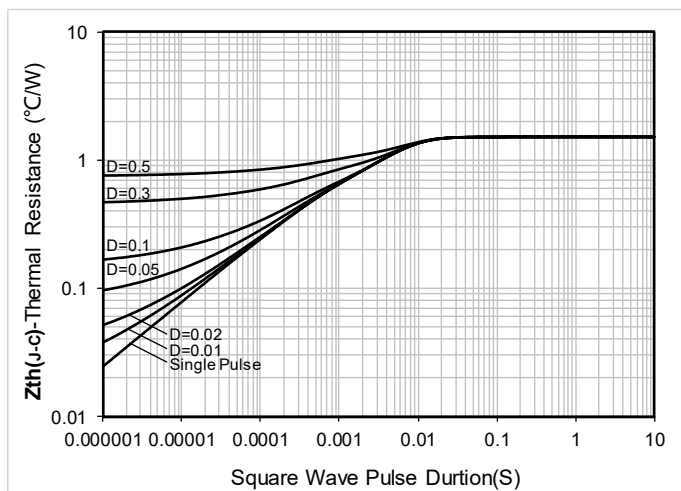


Figure 13. Maximum Transient Thermal Impedance

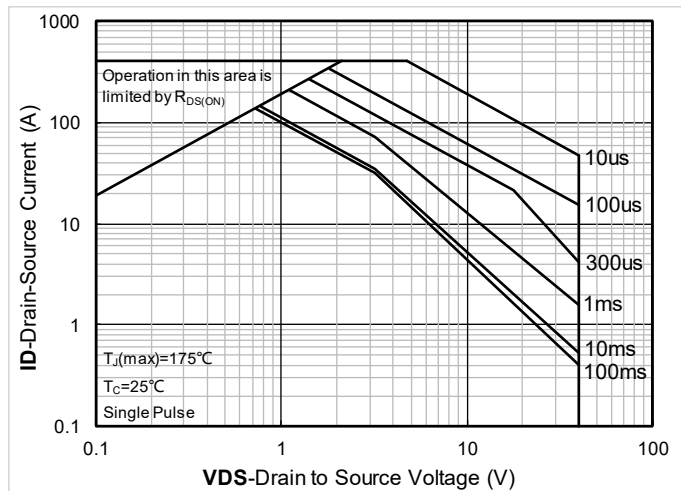


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

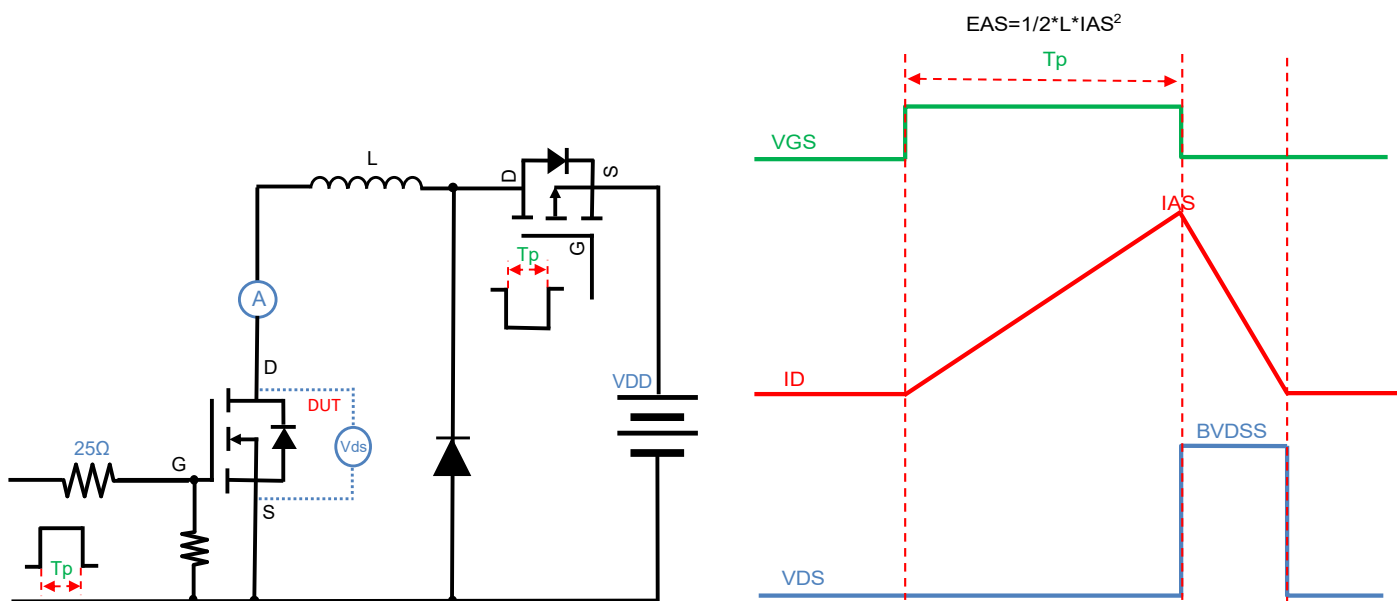


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

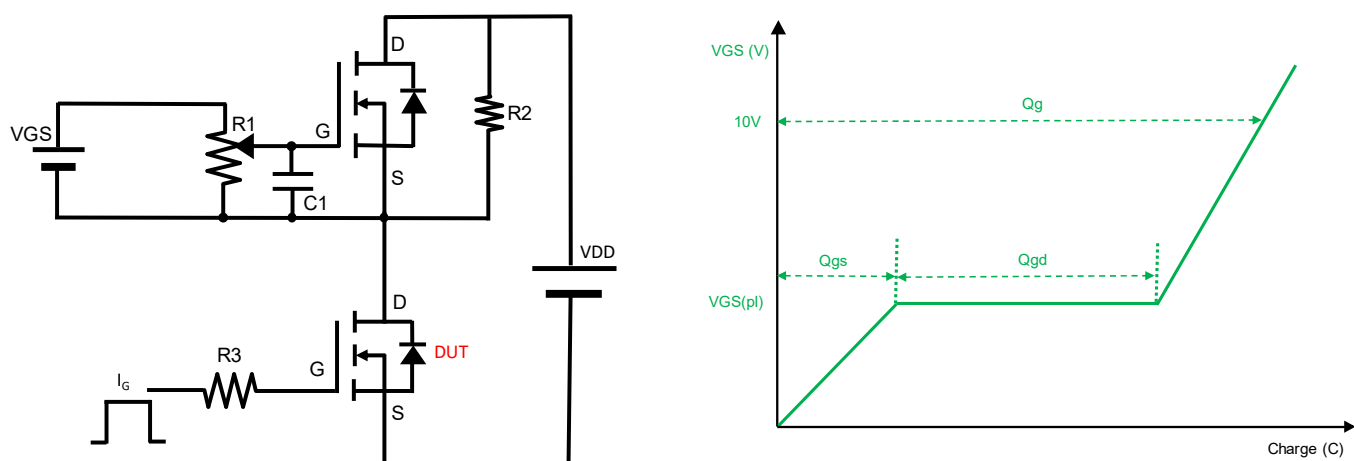


Figure B. Gate Charge Test Circuit & Waveform

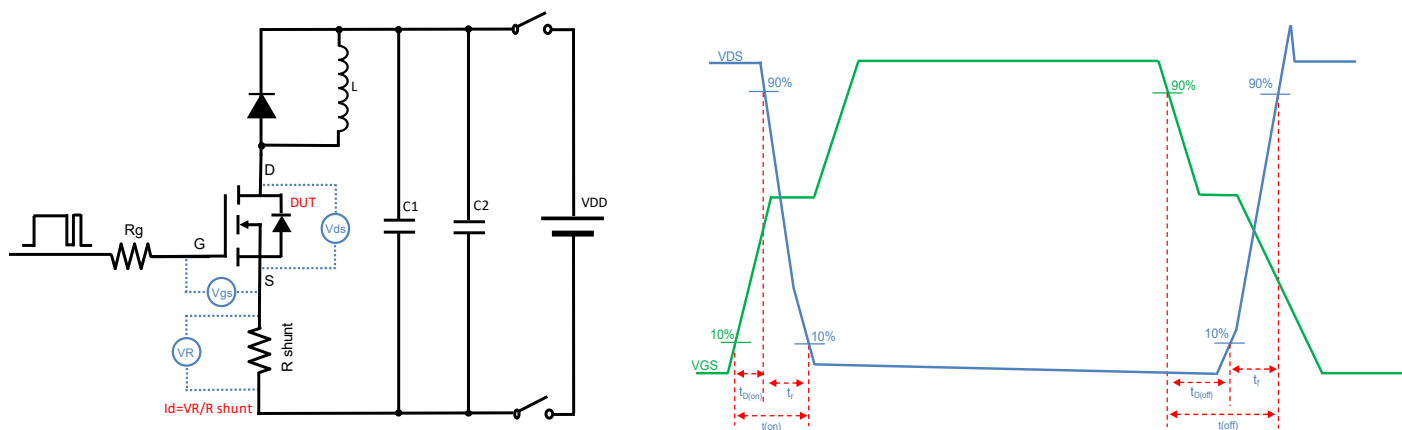


Figure C. Resistive Switching Test Circuit & Waveform

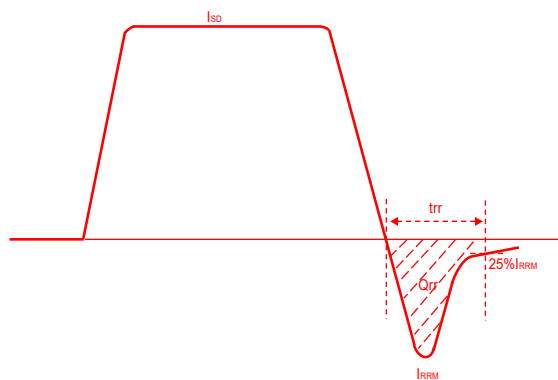
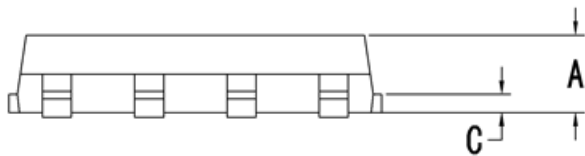
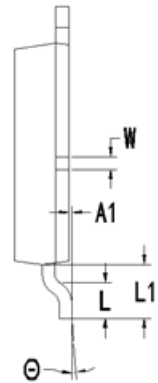
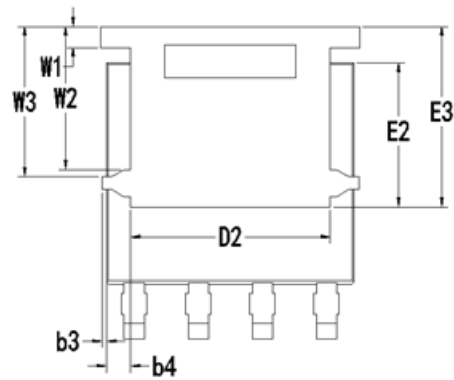
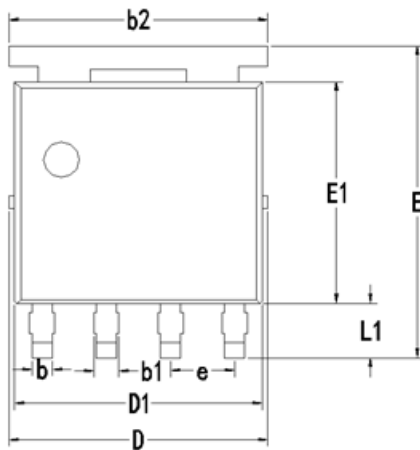


Figure D. Diode Recovery Test Circuit & Waveform



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■ LFPAK56W-8L-A-1.04MM Package information



Note:

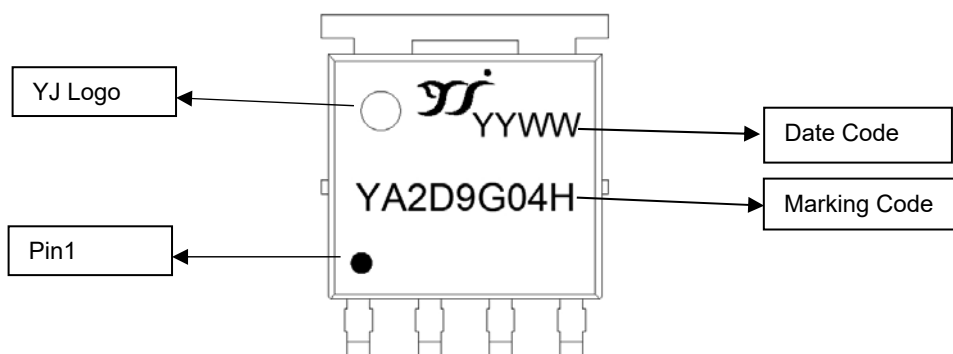
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.04	1.07
A1	0.00	0.06	0.127
b	0.33	0.41	0.48
b1	0.44	0.51	0.58
b2	4.80	4.90	5.00
b3	-	0.094	-
b4	-	0.47	-
c	0.20	0.254	0.30
D	5.00	5.10	5.25
D1	4.80	4.90	5.00
D2	3.86	3.96	4.06
E	6.05	6.15	6.25
E1	4.27	4.37	4.47
E2	2.75	2.85	2.95
E3	3.46	3.56	3.66
e	1.27		
L	0.62	0.72	0.82
L1	0.92	1.07	1.22
W	-	0.23 BSC	-
W1	-	0.41 BSC	-
W2	-	2.82 BSC	-
W3	-	2.96 BSC	-
Θ	0°		10°



YJYA2D9G04HHQ

■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YA2D9G04H is marking code, YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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