

Features:

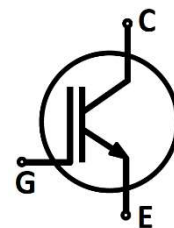
- 650V Trench & field stop technology
- Low switching losses
- Low collector-emitter saturation voltage V_{cesat}
- Positive Temperature coefficient

Recommended for:

Discrete components

Applications:

UPS
EV-Charging
String inverter
Welding



Mechanical parameters

Die size (including scribe lane 60um)	$L \times W$	4.46×5.06	mm ²
Emitter pad size	$L \times W$	See chip drawing	mm ²
Gate pad size	$L \times W$	0.35×0.5	mm ²
Scribe lane		60	μm
Silicon thickness		60	μm
Wafer size		200	mm
Maximum possible chips per wafer		1224	
Passivation frontside		Polyimide	
Pad Metallization	AlCu	4	μm
Backside Metallization	Al / Ti / Ni / Ag	1.7	μm

Maximum Ratings

Parameters	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	650	V
Pulsed collector current, t_p limited by $T_{vj\ max}^1$	$I_{C\ puls}$	300	A
Gate-emitter voltage	V_{GE}	±20	V
Operating junction temperature	$T_{vj\ op}$	-40~175	°C
Storage temperature	T_{stg}	-40~150	°C

Static Characteristic ($T_{vj}=25^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_{GE}=15V$, $I_C=25A$	-	1.05	-	V
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C=0.66mA$, $V_{CE}=V_{GE}$	-	4.0	-	V
Collector-emitter leakage	I_{CES}	$V_{CE}=650V$, $V_{GE}=0V$	-	-	10	μA
Gate-emitter leakage	I_{GES}	$V_{CE}=0V$, $V_{GE}=20V$	-	-	100	nA

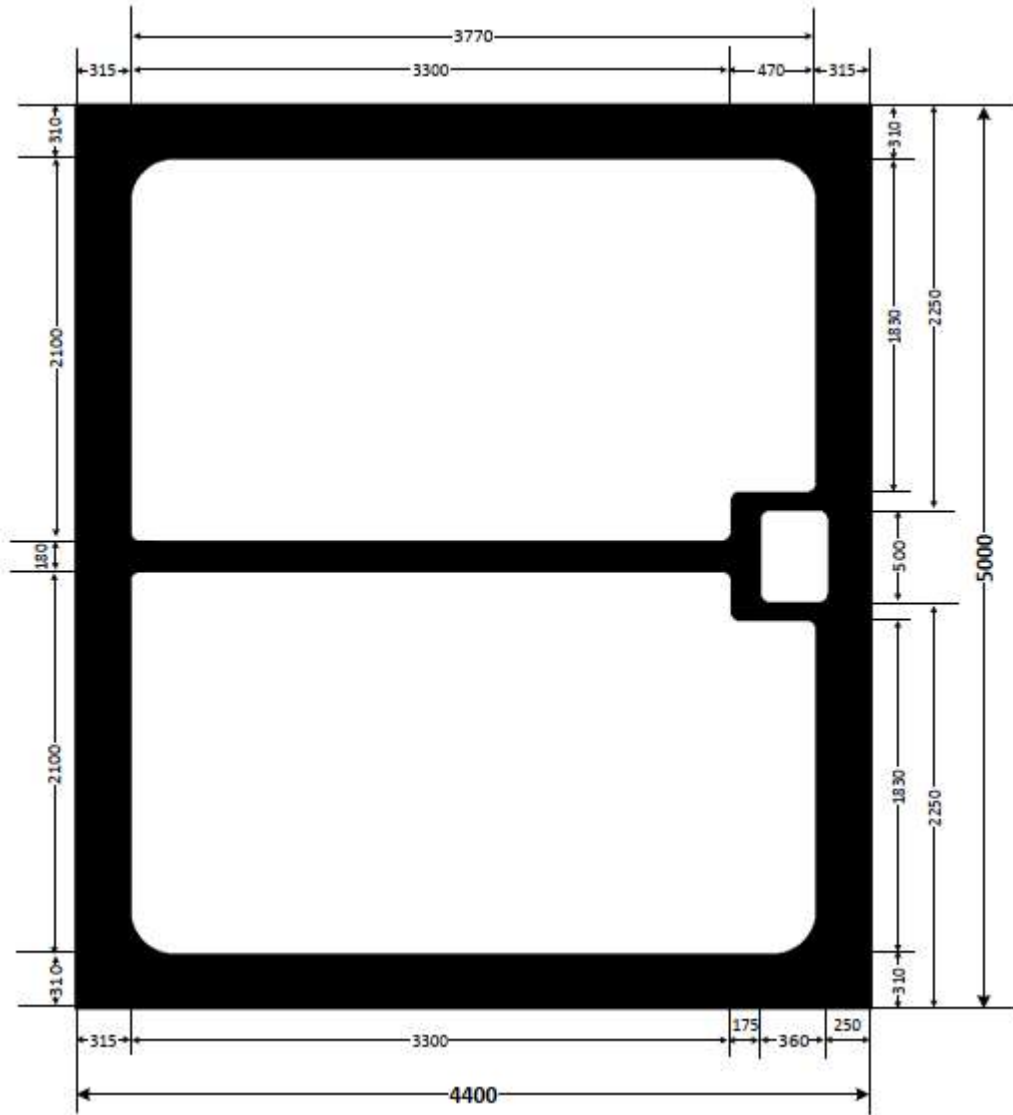
¹ Not subject to production test - verified by design/characterization.

Electrical Characteristic ¹

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$T_{vj}=25^{\circ}\text{C}$	$V_{CE(sat)}$	$V_{GE}=15\text{V}, I_C=75\text{A}$	-	1.40	-	V
	$T_{vj}=175^{\circ}\text{C}$				1.70		V
Input capacitance		C_{ies}	$V_{CE}=25\text{V},$ $V_{GE}=0\text{V}, f=100\text{kHz},$ $T_{vj}=25^{\circ}\text{C}$	-	8600	-	pF
Reverse transfer capacitance		C_{res}		-	48	-	pF
Turn-on delay time (inductive load)	$T_{vj}=25^{\circ}\text{C}$	t_{don}	$V_{CC}=400\text{V},$ $V_{GE}=15\text{V}/0\text{V},$ $R_g=10\Omega, I_C=75\text{A}$	-	64	-	ns
	$T_{vj}=175^{\circ}\text{C}$			-	64	-	ns
Rise time (inductive load)	t_r	-		84	-	ns	
		-		84	-	ns	
Turn-off delay time (inductive load)	t_{doff}	-		233	-	ns	
		-		235	-	ns	
Fall time (inductive load)	t_f	-		105	-	ns	
		-		106	-	ns	

¹ Not subject to production test - verified by design/characterization.

Chip Drawing –scribe lane 60um not included (unit: μm)



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