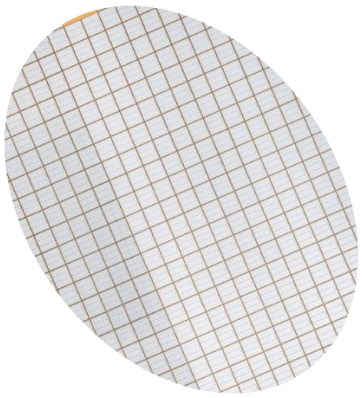
DATASHEET

SIS0100C120i20

I20 fine pattern IGBT, 8.8mm x 8.8mm



Symbolic picture

V_{CE} = 1200 V
I_C = 100 A

- *i20* ultra-low loss fine pattern Trench IGBT chipset
- positive temperature coefficient
- easy paralleling

Maximum ratings[1]

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Collector-emitter voltage	V_{CES}	V_{GE} = 0 V, T_{vj} >/= 25 °C		1200	V
DC collector current	I_C			100	A
Peak collector current	I_{CM}	t_p limited by $T_{vj\,max}$		200	A
Gate-emitter voltage	V_{GES}		-20	20	V
Junction temperature	T_{vj}		-40	175	°C
Junction operating temperature	$T_{vj(op)}$		-40	175	°C
Short circuit[2]	t_{sc}	V_{GE} = 15V, V_{CC} = 800V, T_{vj} = 175°C[3]		10	µs

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[1] Maximum rated values indicate limits beyond which damage to the device may occur per IEC 60747
[2] Not subject to production test, capability depending on module design
[3] Short circuit performance at high temperature requires suitable die assembly process

IGBT[4]

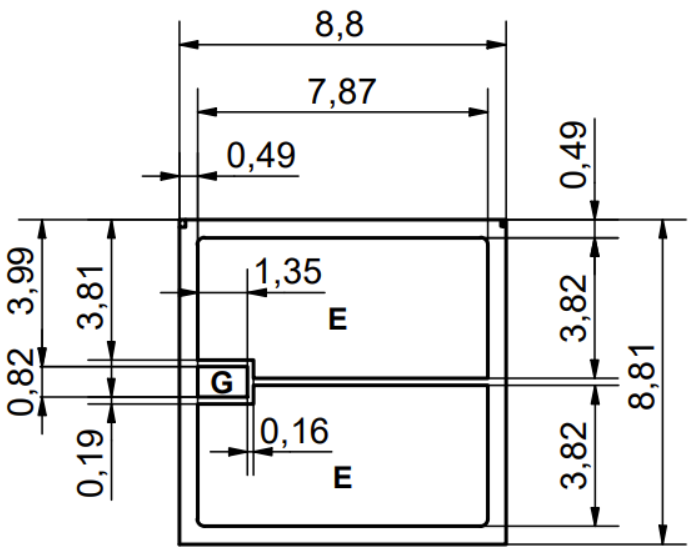
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Collector(-emitter) breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0 V, I_C = 0.25mA, T_{vj} = 25°C		1200			V
Collector-emitter saturation voltage [5]	V_{CEsat}	I_c = 100 A, V_{GE} = 15 V	T_{vj} = 25 °C		1.7		V
			T_{vj} = 125 °C		2.05		V
			T_{vj} = 175 °C		2.2		V
Collector cut-off current	I_{CES}	V_{CE} = 1200 V, V_{GE} = 0 V	T_{vj} = 25 °C			1.0	µA
Gate leakage current	I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V		-0.5		0.5	µA
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C = 5 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		5	5.8	7.5	V
Gate charge	Q_G	I_C = 200 A, V_{CE} = 600 V, V_{GE} = -15 V .. 15 V			0.75		µC
Input capacitance	C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 100 kHz, T_{vj} = 25 °C			5.8		nF
Output capacitance	C_{oes}				0.307		nF
Reverse tansfer capacitance	C_{res}				0.253		nF
Internal gate resistor	R_{Gint}	Per switch			6.8		Ω
Turn-on delay time	$t_{d(on)}$	V_{CC} = 600 V, I_C = 100 A, R_G = 4 Ω, V_{GE} = ± 15 V	T_{vj} = 25 °C		115		ns
			T_{vj} = 125 °C		128		ns
			T_{vj} = 175 °C		1136		ns
Rise time	t_r		T_{vj} = 25 °C		43		ns
			T_{vj} = 125 °C		46		ns
			T_{vj} = 175 °C		548		ns
Turn-off delay time	$t_{d(off)}$	V_{CC} = 600 V, I_C = 100 A, R_G = 11 Ω, V_{GE} = ± 15 V	T_{vj} = 25 °C		430		ns
			T_{vj} = 125 °C		525		ns
			T_{vj} = 175 °C		573		ns
Fall time	t_f		T_{vj} = 25 °C		308		ns
			T_{vj} = 125 °C		397		ns
			T_{vj} = 175 °C		430		ns
Turn-on switching energy	E_{on}	V_{CC} = 600 V, I_C = 100 A, R_G = 4 Ω, V_{GE} = ± 15 V	T_{vj} = 25 °C		6		mJ
			T_{vj} = 125 °C		8.5		mJ
			T_{vj} = 175 °C		10		mJ
Turn-off switching energy	E_{off}	V_{CC} = 600 V, I_C = 100 A, R_G = 11 Ω, V_{GE} = ± 15 V	T_{vj} = 25 °C		11		mJ
			T_{vj} = 125 °C		14.5		mJ
			T_{vj} = 175 °C		16		mJ
Short circuit current	I_{SC}	t_{pcs} ≤ 10 µs, V_{GE} = 15 V, T_{vj} = 175 °C, V_{CC} = 800 V, $v_{CEM\ Chip}$ ≤ 1200 V			251		A

[4] Characteristic values according to IEC 60747-9

Mechanical properties

PARAMETER		UNIT 单位
Die size	8.8*8.81	mm^2
Gate pad size	1.3 x 0.8	mm^2
Thickness	135	µm
Wafer diameter	300	mm
Maximum chips per wafer	784	pcs
Frontside passivation	Polyimide	
Frontside metal (pads)	Al Cu, 5000nm	
Backside metal	Al Ni Ag System, 1100nm	

Chip drawing



This is an electrostatic sensitive device.