DATASHEET

SIS0200C120i21

i21 fine pattern IGBT, 12.8 mm x 12.1 mm

V_{CE} = 1200 V
I_C = 200 A

- *i21* ultra-low loss fine pattern Trench IGBT chipset
- Optimized for switching at high stray inductance
- positive temperature coefficient
- easy paralleling

Maximum ratings[1]

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Collector-emitter voltage	V_{CES}	V_{GE} = 0 V, T_{vj} ≥ 25 °C		1200	V
DC collector current	I_C			200	A
Peak collector current	I_{CM}	t_p limited by $T_{vj\,max}$		400	A
Gate-emitter voltage	V_{GES}		-20	20	V
Junction temperature	T_{vj}		-40	175	°C
Junction operating temperature	$T_{vj(op)}$		-40	175	°C
Short circuit[2]	t_{sc}	V_{GE} = 15V, V_{CC} = 800V, T_{vj} = 175°C[3]		8	µs

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[1] Maximum rated values indicate limits beyond which damage to the device may occur per IEC 60747
[2] Not subject to production test, capability depending on module design
[3] Short circuit performance at high temperature requires suitable die assembly process

IGBT[4]

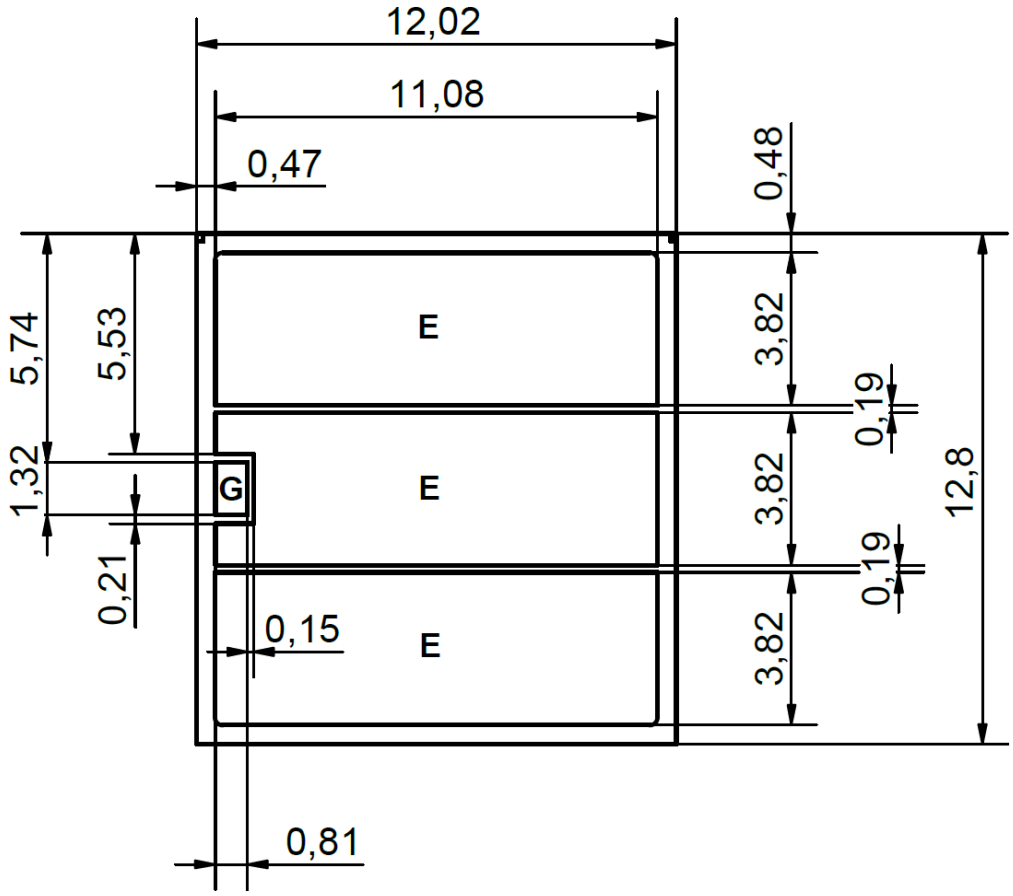
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Collector(-emitter) breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0 V, I_C = 0.2 mA, T_{vj} = 25 °C		1200			V
Collector-emitter saturation voltage [5]	V_{CEsat}	I_c = 200 A, V_{GE} = 15 V	T_{vj} = 25 °C		1.48		V
			T_{vj} = 125 °C		1.68		V
			T_{vj} = 175 °C		1.8		V
Collector cut-off current	I_{CES}	V_{CE} = 1200 V, V_{GE} = 0 V	T_{vj} = 25 °C			1.0	µA
Gate leakage current	I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V		-0.5		0.5	µA
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C = 10 mA, V_{CE} = V_{GE}, T_{vj} = 25°C			5.8		V
Gate charge	Q_G	I_C = 200 A, V_{CE} = 600 V, V_{GE} = -15 V .. 15 V			1.9		µC
Input capacitance	C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz, T_{vj} = 25 °C			13.3		nF
Output capacitance	C_{oes}				0.66		nF
Reverse tansfer capacitance	C_{res}				0.53		nF
Internal gate resistor	R_{Gint}	Per switch			4.0		Ω
Turn-on delay time	$t_{d(on)}$	V_{CC} = 600 V, I_C = 200 A, R_G = 4.5 Ω, V_{GE} = ± 15 V	T_{vj} = 25 °C		175		ns
			T_{vj} = 125 °C		205		ns
			T_{vj} = 175 °C		220		ns
Rise time	t_r		T_{vj} = 25 °C		60		ns
			T_{vj} = 125 °C		67		ns
			T_{vj} = 175 °C		75		ns
Turn-off delay time	$t_{d(off)}$	V_{CC} = 600 V, I_C = 200 A, R_G = 4.5 Ω, V_{GE} = ± 15 V	T_{vj} = 25 °C		550		ns
			T_{vj} = 125 °C		653		ns
			T_{vj} = 175 °C		675		ns
Fall time	t_f		T_{vj} = 25 °C		352		ns
			T_{vj} = 125 °C		475		ns
			T_{vj} = 175 °C		498		ns
Turn-on switching energy	E_{on}	V_{CC} = 600 V, I_C = 200 A, R_G = 4.5 Ω, V_{GE} = ± 15 V Diode: SID0250C120d20	T_{vj} = 25 °C		16		mJ
			T_{vj} = 125 °C		25		mJ
			T_{vj} = 175 °C		31		mJ
Turn-off switching energy	E_{off}	V_{CC} = 600 V, I_C = 200 A, R_G = 4.5 Ω, V_{GE} = ± 15 V	T_{vj} = 25 °C		30		mJ
			T_{vj} = 125 °C		39		mJ
			T_{vj} = 175 °C		43		mJ
Short circuit current	I_{SC}	t_{pcs} ≤ 8 µs, V_{GE} = 15 V, T_{vj} = 175 °C, V_{CC} = 800 V, $v_{CEM\ Chip}$ ≤ 1200 V			750		A

[4] Characteristic values according to IEC 60747-9

Mechanical properties[6]

PARAMETER		UNIT
Die size	12.8 x 12.02	mm^2
Gate pad size	1.3 x 0.8	mm^2
Thickness	145	µm
Wafer diameter	300	mm
Maximum chips per wafer	386	pcs
Frontside passivation	Polyimide	
Frontside metal (pads)	Al Cu, 5000nm	
Backside metal	Al Ni Ag System, 1100nm	

Chip drawing



This is an electrostatic sensitive device.