

DATASHEET

SIS0200C175i20

I20 fine pattern IGBT, 15.8mm x 12.1mm



$V_{CE} = 1700\text{ V}$

$I_C = 200\text{ A}$

- i20 ultra-low loss fine pattern Trench IGBT chipset
- positive temperature coefficient
- easy paralleling

Maximum ratings¹

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Collector-emitter voltage	V_{CES}	$V_{GE} = 0\text{ V}$, $T_{vj} \geq 25\text{ °C}$		1700	V
DC collector current	I_C			200	A
Peak collector current	I_{CM}	t_p limited by $T_{vj\text{ max}}$		400	A
Gate-emitter voltage	V_{GES}		-20	20	V
Junction temperature	T_{vj}		-40	175	°C
Junction operating temperature	$T_{vj(op)}$		-40	175	°C
Short circuit ²	t_{sc}	$V_{GE} = 15\text{ V}$, $V_{CC} = 1200\text{ V}$, $T_{vj} = 175\text{ °C}$ ³		10	µs



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¹ Maximum rated values indicate limits beyond which damage to the device may occur per IEC 60747

² Not subject to production test, capability depending on module design

³ Short circuit performance at high temperature requires suitable die assembly process

IGBT⁴

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Collector(-emitter) breakdown voltage	V _{(BR)CES}	V _{GE} = 0 V, I _C = 0.25mA, T _{vj} = 25°C		1700			V
Collector-emitter saturation voltage ⁵	V _{CEsat}	I _C = 200 A, V _{GE} = 15 V	T _{vj} = 25 °C		1.65		V
			T _{vj} = 125 °C		1.85		V
			T _{vj} = 175 °C		2.05		V
Collector cut-off current	I _{CES}	V _{CE} = 1700 V, V _{GE} = 0 V	T _{vj} = 25 °C			1.0	μA
Gate leakage current	I _{GES}	V _{CE} = 0 V, V _{GE} = ±20 V		-0.5		0.5	μA
Gate-emitter threshold voltage	V _{GE(th)}	I _C = 12 mA, V _{CE} = V _{GE} , T _{vj} = 25°C		5	6.15	7.5	V
Gate charge	Q _G	I _C = 200 A, V _{CE} = 900 V, V _{GE} = -15 V .. 15 V			1.5		μC
Input capacitance	C _{ies}	V _{CE} = 25 V, V _{GE} = 0 V, f = 100 kHz, T _{vj} = 25 °C			15.3		nF
Output capacitance	C _{oes}				0.89		nF
Reverse tansfer capacitance	C _{res}				0.47		nF
Internal gate resistor	R _{Gint}	Per switch			4.2		Ω
Turn-on delay time	t _{d(on)}	V _{CC} = 900 V, I _C = 200 A, R _G = 4.5 Ω, V _{GE} = ± 15 V	T _{vj} = 25 °C		105		ns
			T _{vj} = 125 °C		130		ns
			T _{vj} = 175 °C		150		ns
Rise time	t _r		T _{vj} = 25 °C		52		ns
			T _{vj} = 125 °C		58		ns
			T _{vj} = 175 °C		62		ns
Turn-off delay time	t _{d(off)}	V _{CC} = 900 V, I _C = 200 A, R _G = 4.5 Ω, V _{GE} = ± 15 V	T _{vj} = 25 °C		590		ns
			T _{vj} = 125 °C		720		ns
			T _{vj} = 175 °C		775		ns
Fall time	t _f		T _{vj} = 25 °C		360		ns
			T _{vj} = 125 °C		570		ns
			T _{vj} = 175 °C		660		ns
Turn-on switching energy	E _{on}	V _{CC} = 900 V, I _C = 200 A, R _G = 4.5 Ω, V _{GE} = ± 15 V Diode: SID0200C175d20	T _{vj} = 25 °C		54		mJ
			T _{vj} = 125 °C		74		mJ
			T _{vj} = 175 °C		87		mJ
Turn-off switching energy	E _{off}	V _{CC} = 900 V, I _C = 200 A, R _G = 4.5 Ω, V _{GE} = ± 15 V	T _{vj} = 25 °C		44		mJ
			T _{vj} = 125 °C		64		mJ
			T _{vj} = 175 °C		72		mJ
Short circuit current	I _{SC}	t _{pcs} ≤ 10 μs, V _{GE} = 15 V, T _{vj} = 175 °C, V _{CC} = 1200 V, V _{CEM Chip} ≤ 1700 V			790		A

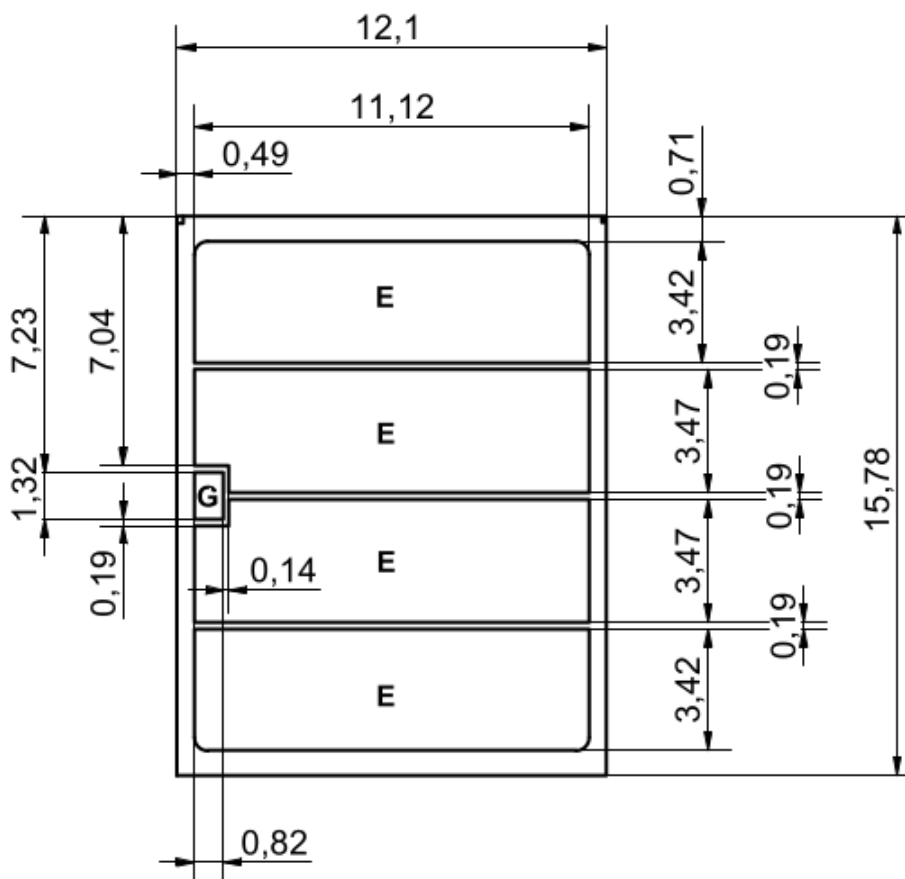
⁴ Characteristic values according to IEC 60747-9



Mechanical properties⁶

PARAMETER		UNIT
Die size	15.78 x 12.1	mm ²
Gate pad size	1.32 x 0.82	mm ²
Thickness	185	μm
Wafer diameter	200	mm
Maximum chips per wafer	126	pcs
Frontside passivation	Polyimide	
Frontside metal (pads)	Al Cu, 5000nm	
Backside metal	Al Ni Ag System, 1100nm	

Chip drawing



This is an electrostatic sensitive device.