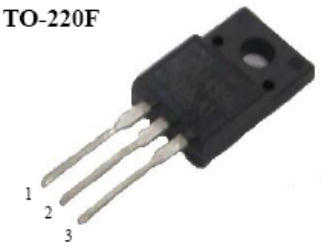
## General Description：

CS3N90FA9R, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

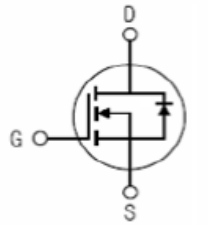
| | | |
|---|---|---|
| $V_{DSS}$ | 900 | V |
| $I_D$ | 3 | A |
| $P_D$($T_C$=25℃) | 32 | W |
| $R_{DS(ON)Typ}$ | 4.8 | Ω |

TO-220F




1. Gate 2. Drain 3. Source

Inner Equivalent Principium Chart




## Features：

- **Fast Switching**
- **Low ON Resistance(Rdson≤5.5Ω)**
- **Low Gate Charge (Typical Data:17.4 nC)**
- **Low Reverse transfer capacitances(Typical: 3.8pF)**
- **100% Single Pulse avalanche energy Test**

## Applications：

Power switch circuit of adaptor and charger.

**Absolute**（Tj= 25℃ unless otherwise specified）：

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage | 900 | V |
| $I_D$ | Continuous Drain Current $T_C$ = 25 °C | 3 | A |
| | Continuous Drain Current $T_C$ = 100 °C | 1.9 | A |
| $I_{DM}$ [a1] | Pulsed Drain Current $T_C$ = 25 °C | 12 | A |
| $V_{GS}$ | Gate-to-Source Voltage | ±30 | V |
| $E_{AS}$ [a2] | Single Pulse Avalanche Energy | 125 | mJ |
| dv/dt [a3] | Peak Diode Recovery dv/dt | 5.0 | V/ns |
| $P_D$ | Power Dissipation $T_C$ = 25 °C | 32 | W |
| | Derating Factor above 25°C | 0.25 | W/℃ |
| $T_J$， $T_{stg}$ | Operating Junction and Storage Temperature Range | 150，−55 to 150 | ℃ |
| $T_L$ | Maximum Temperature for Soldering | 300 | ℃ |

**Electrical Characteristics**（Tj= 25℃ unless otherwise specified）：

| **OFF Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $V_{DSS}$ | Drain to Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250μA | 900 | -- | -- | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Bvdss Temperature Coefficient | ID=250uA,Reference25℃ | -- | 0.9 | -- | V/℃ |
| $I_{DSS}$ | Drain to Source Leakage Current | $V_{DS}$ =900V, $V_{GS}$= 0V, Tj = 25℃ | -- | -- | 25 | μA |
| | | $V_{DS}$ =720V, $V_{GS}$= 0V, Tj = 125℃ | -- | -- | 250 | μA |
| $I_{GSS(F)}$ | Gate to Source Forward Leakage | $V_{GS}$ =+30V | -- | -- | 100 | nA |
| $I_{GSS(R)}$ | Gate to Source Reverse Leakage | $V_{GS}$ =-30V | -- | -- | -100 | nA |

| **ON Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $R_{DS(ON)}$ | Drain-to-Source On-Resistance | $V_{GS}$=10V,$I_D$=1.5A | -- | 4.8 | 5.5 | Ω |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 2.0 | -- | 4.0 | V |
| Pulse width tp≤300μs,δ≤2% | | | | | | |

| **Dynamic Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $g_{fs}$ | Forward Transconductance | $V_{DS}$=15V, $I_D$ =1.5A | -- | 9.5 | -- | S |
| $R_g$ | Gate resistance | f = 1.0MHz | -- | 3.3 | -- | Ω |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0V $V_{DS}$ = 25V f = 1.0MHz | -- | 561 | -- | PF |
| $C_{oss}$ | Output Capacitance | | -- | 47 | -- | |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 3.8 | -- | |

| **Resistive Switching Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $t_{d(ON)}$ | Turn-on Delay Time | $I_D$ =3A $V_{DD}$ = 450V $V_{GS}$ = 10V $R_G$ =10Ω | -- | 12.8 | -- | ns |
| tr | Rise Time | | -- | 18 | -- | |
| $t_{d(OFF)}$ | Turn-Off Delay Time | | -- | 32.8 | -- | |
| $t_f$ | Fall Time | | -- | 39.6 | -- | |
| $Q_g$ | Total Gate Charge | $I_D$ =3A $V_{DD}$ =630V $V_{GS}$ = 10V | -- | 17.4 | -- | nC |
| $Q_{gs}$ | Gate to Source Charge | | -- | 2.3 | -- | |
| $Q_{gd}$ | Gate to Drain (“Miller”)Charge | | -- | 10 | -- | |
| Vp | Platform Voltage | | | 4.9 | | V |

| Source-Drain Diode Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $I_S$ | Continuous Source Current (Body Diode) | $T_C$ = 25 °C | -- | -- | 3 | A |
| $I_{SM}$ | Maximum Pulsed Current (Body Diode) | | -- | -- | 12 | A |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=3A,$V_{GS}$=0V | -- | -- | 1.5 | V |
| $T_{rr}$ | Reverse Recovery Time | $I_S$=10.0A,$T_j$ = 25°C<br>$dI_F/dt$=100A/us,<br>$V_{GS}$=0V | -- | 503 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 1697 | -- | nC |
| $I_{rrm}$ | Reverse Recovery Current | | -- | 8.1 | -- | A |
| Pulse width tp≤300μs,δ≤2% | | | | | | |

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | 3.88 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | 62.5 | °C/W |

[a1]: Repetitive rating; pulse width limited by maximum junction temperature

[a2]: L=10mH, $I_D$=5A, Start $T_J$=25°C

[a3]: $I_{SD}$ =3A,di/dt ≤100A/us,$V_{DD}$≤$BV_{DS,}$ Start $T_J$=25°C

## Characteristics Curve:

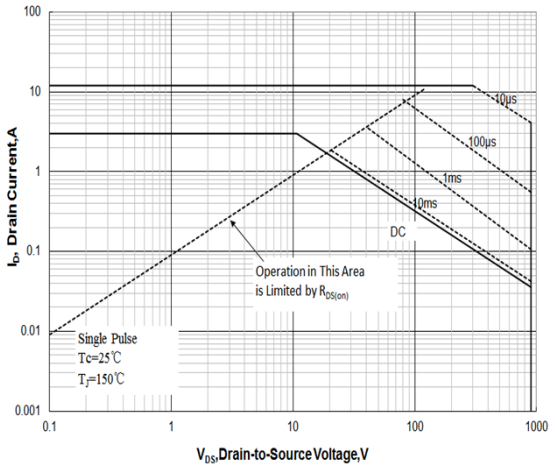



Figure 1 Maximum Forward Bias Safe Operating Area

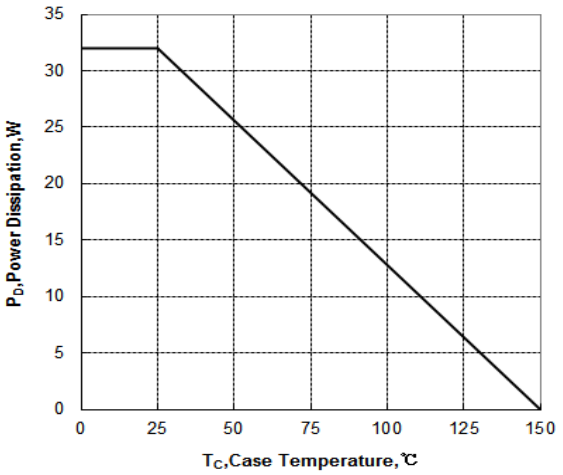



Figure 2 Maximum Power dissipation vs Case Temperature

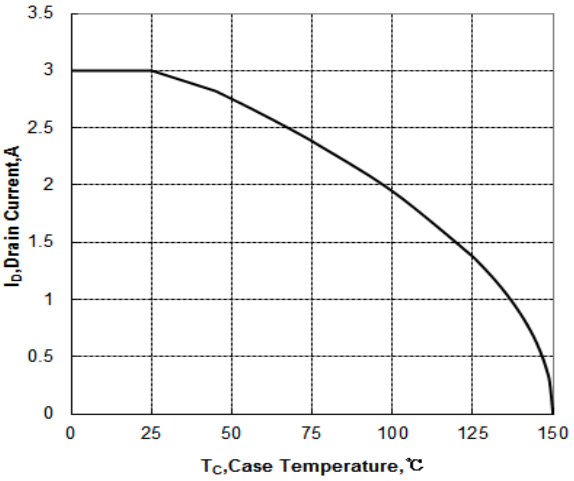



Figure 3 Maximum Continuous Drain Current vs Case

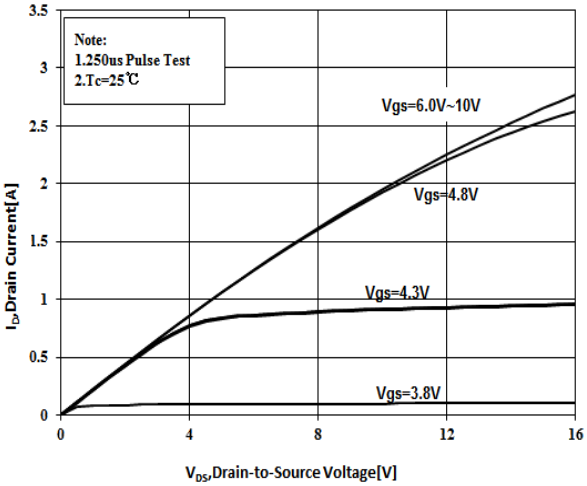



Figure 4 Typical Output Characteristics

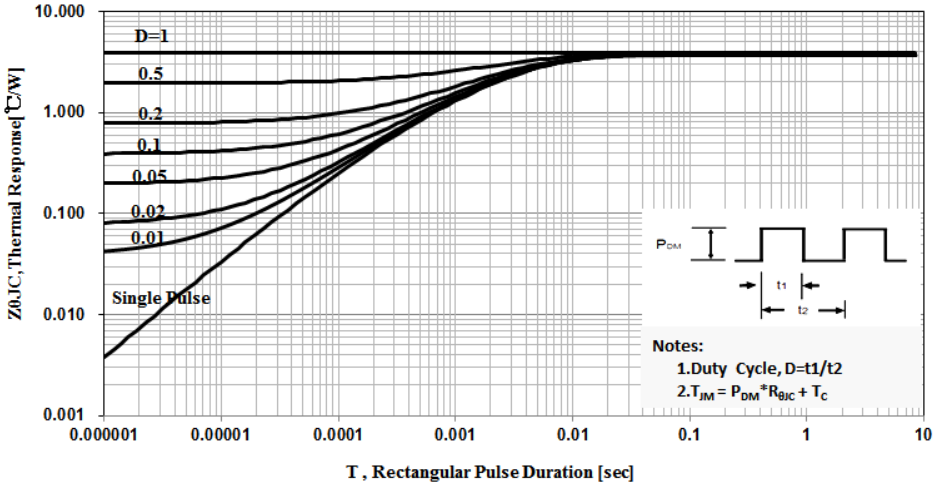



Figure 5 Maximum Effective Thermal Impedance , Junction to Case

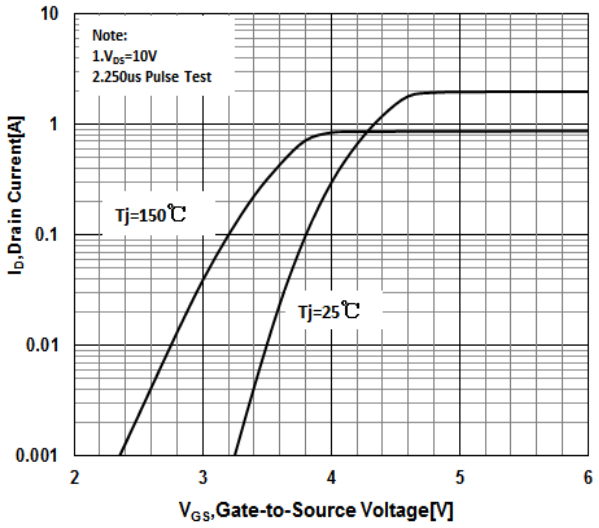



Figure 6 Typical Transfer Characteristics

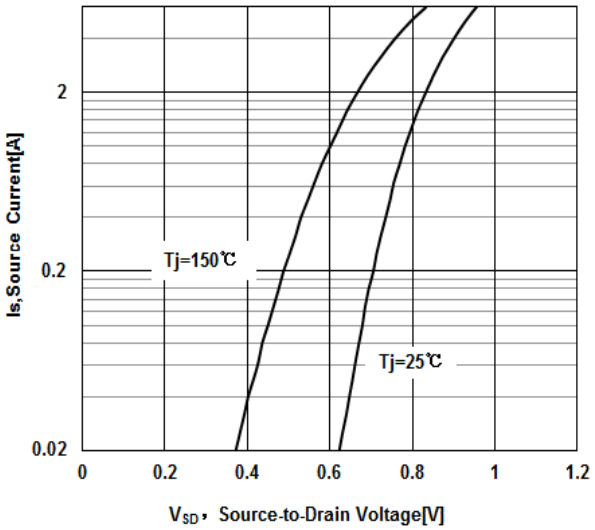



Figure 7 Typical Body Diode Transfer Characteristics

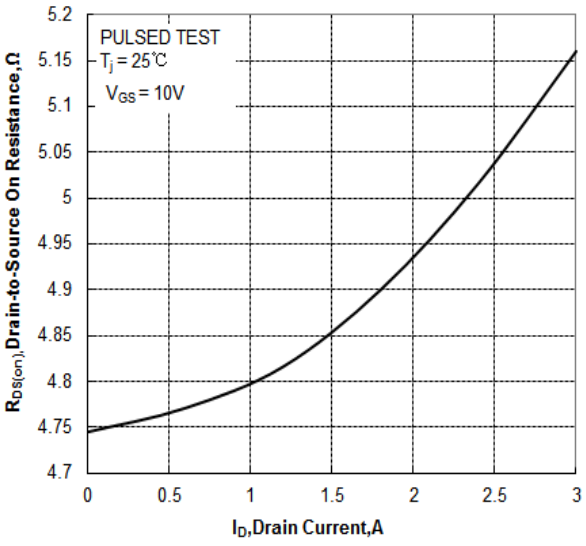



Figure 8 Typical Drain to Source ON Resistance vs Drain Current

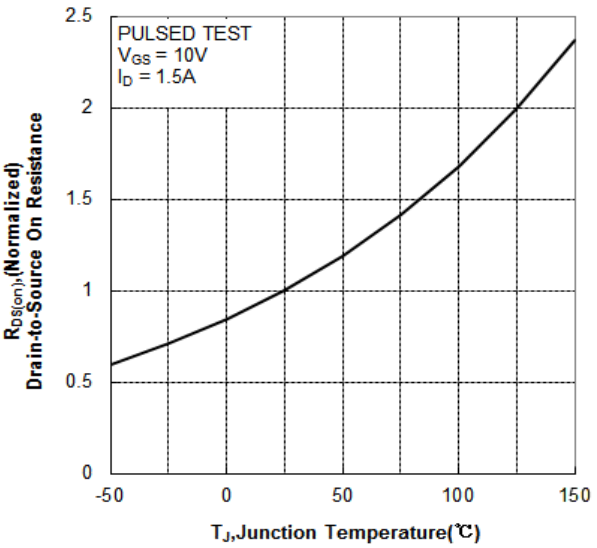



Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

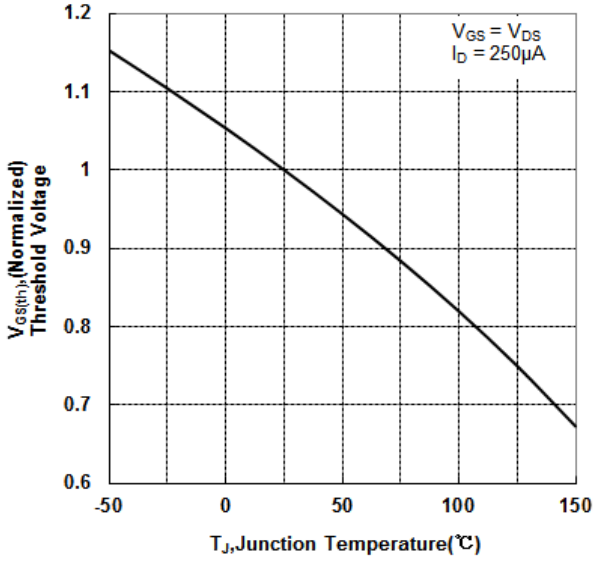



Figure 10 Typical Theshold Voltage vs Junction Temperature

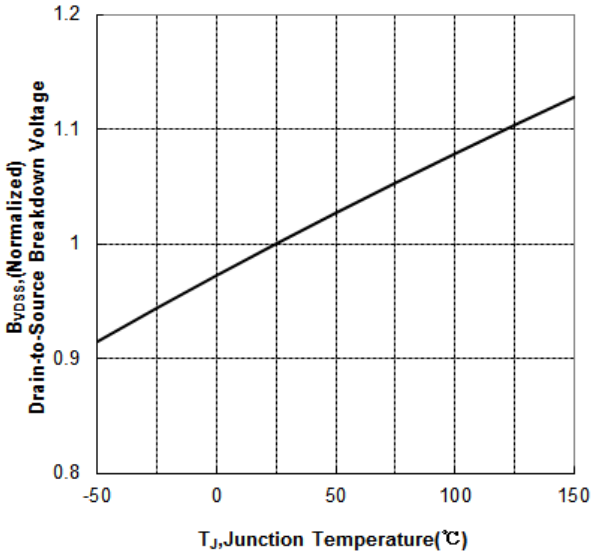



Figure 11 Typical Breakdown Voltage vs Junction Temperature

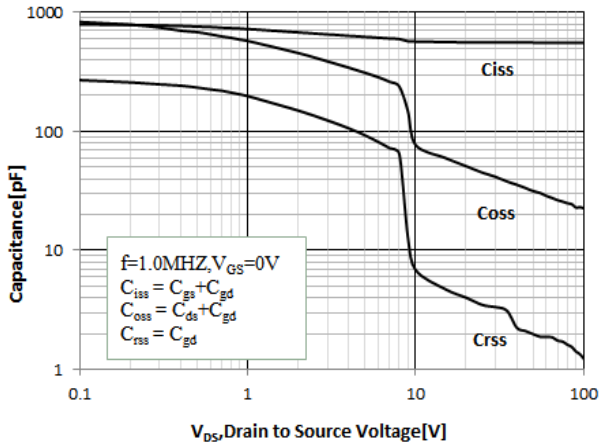



Figure 12 Typical Capacitance vs Drain to Source Voltage

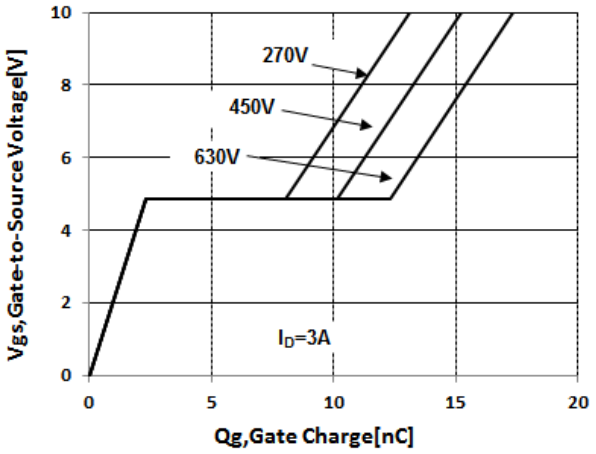



Figure 13 Typical Gate Charge vs Gate to Source Voltage

## Test Circuit and Waveform

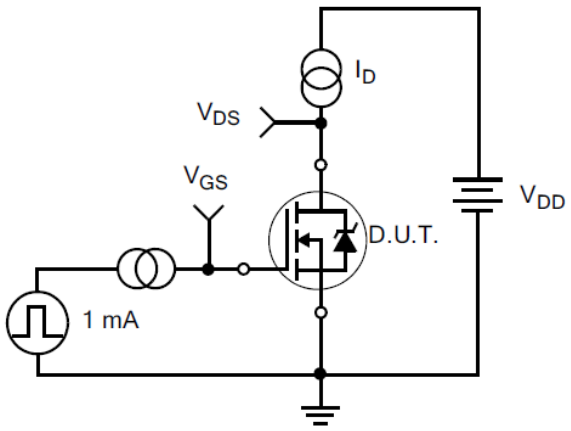



Figure 14. Gate Charge Test Circuit

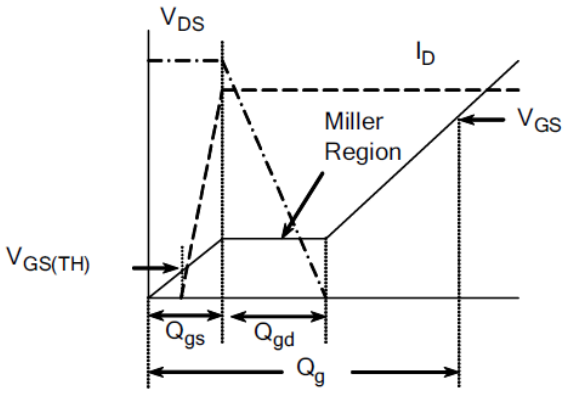



Figure 15. Gate Charge Waveforms

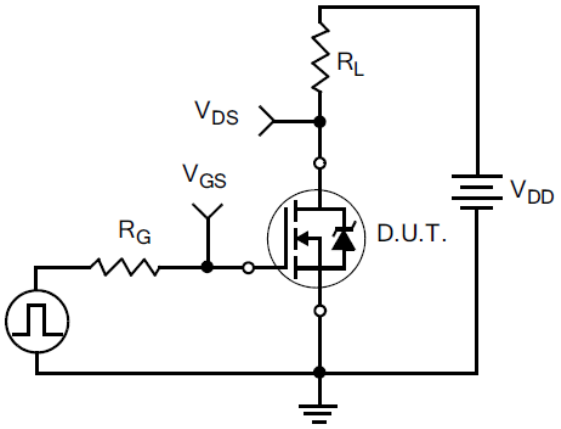



Figure 16. Resistive Switching Test Circuit

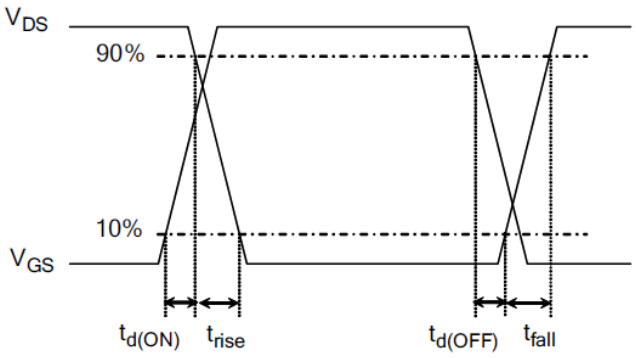



Figure 17. Resistive Switching Waveforms

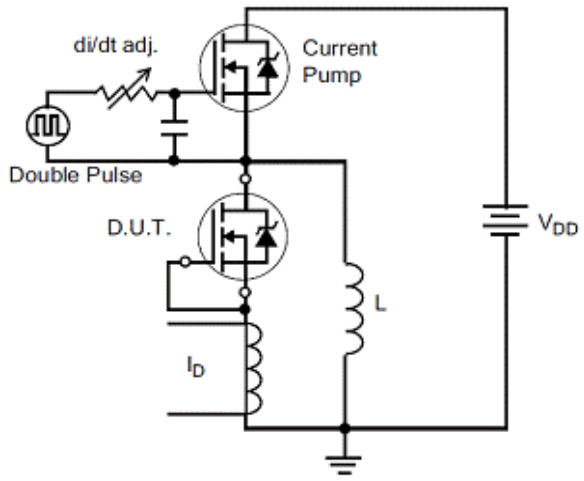



Figure 18. Diode Reverse Recovery Test Circuit

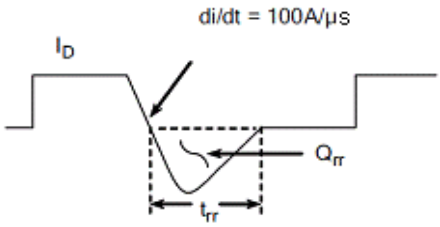



Figure 19. Diode Reverse Recovery Waveform

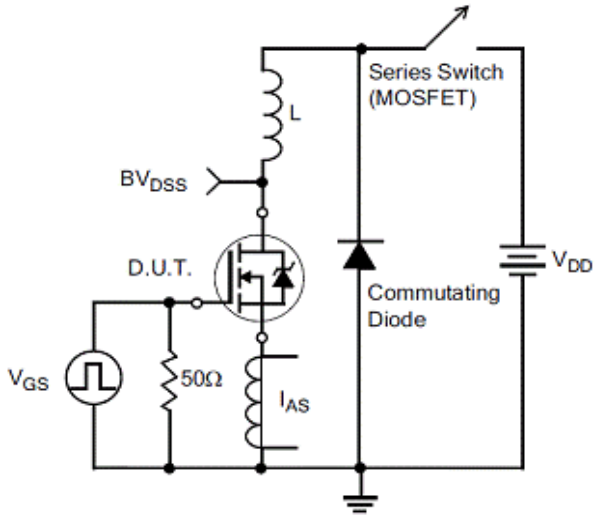



Figure20.Unclamped Inductive Switching Test Circuit

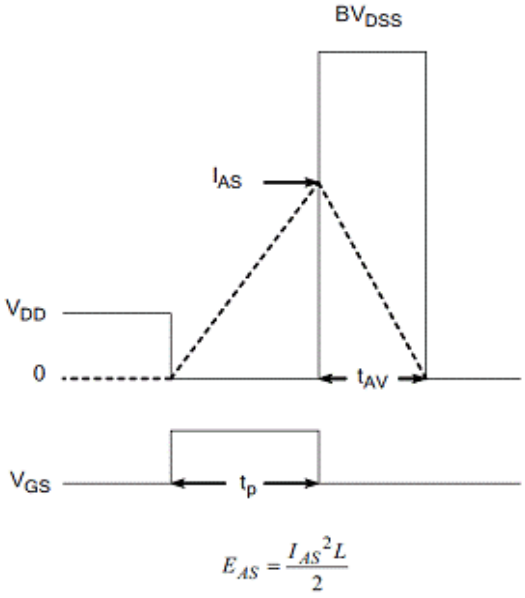
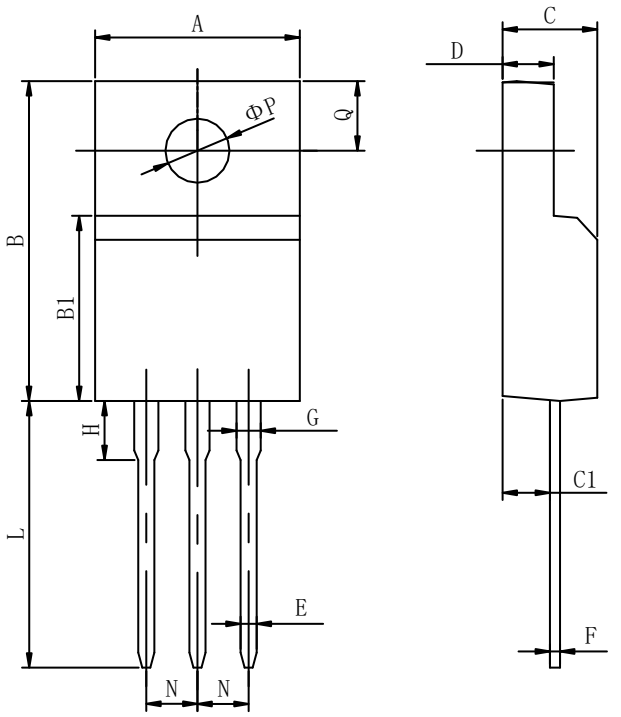



Figure21.Unclamped Inductive Switching Waveform

## Package Information：




| Items | Values(mm) | |
|---|---|---|
| | MIN | MAX |
| A | 9.60 | 10.4 |
| B | 15.4 | 16.2 |
| B1 | 8.90 | 9.50 |
| C | 4.30 | 4.90 |
| C1 | 2.10 | 3.00 |
| D | 2.40 | 3.00 |
| E | 0.60 | 1.00 |
| F | 0.30 | 0.60 |
| G | 1.12 | 1.42 |
| H | 3.40 | 3.80 |
| L* | 12.0 | 14.0 |
| N | 2.34 | 2.74 |
| Q | 3.15 | 3.55 |
| ΦP | 2.90 | 3.30 |

*adjustable

TO-220F Package

## Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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| Revison History | | |
|---|---|---|
| Revision | Date | Major changes |
| 1.0 | 2026/4/28 | Initial release |