NCE N-Channel Super Trench III Power MOSFET

Description

The NCEAP022NH40AQU uses **Super Trench III** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

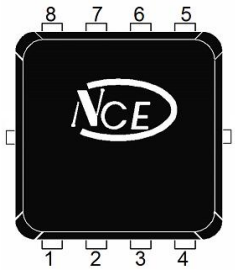
Application

- Automotive application
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

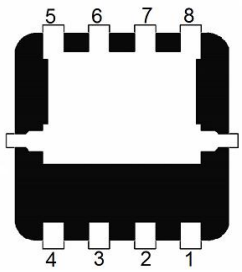
General Features

- V_{DS} =40V,I_D =145A
  $R_{DS(ON)}$=2.0mΩ (typical) @ V_{GS}=10V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested
- 100% ΔVds tested
- **AEC-Q101 qualified**

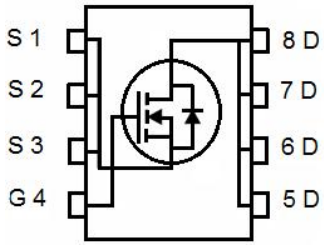
PDFN3.3X3.3-8L



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AP022NH40AQU	NCEAP022NH40AQU	PDFN3.3X3.3-8L	Ø330mm	12mm	5000units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	145	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	102	A
Pulsed Drain Current	I_{DM}	580	A
Maximum Power Dissipation	P_D	99	W
Derating factor		0.66	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	241	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	1.51	℃/W
Thermal Resistance,Junction-to-Ambient (Note 4)	$R_{\theta JA}$	60	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	2.0	2.6	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A	-	50	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V, F=1.0MHz	-	2290	-	pF
Output Capacitance	C_{oss}		-	585	-	pF
Reverse Transfer Capacitance	C_{rss}		-	35	-	pF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V,I_D=20A V_{GS}=10V,R_G=1.6Ω	-	10	-	nS
Turn-on Rise Time	t_r		-	60	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	nS
Turn-Off Fall Time	t_f		-	12	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=20A, V_{GS}=10V	-	38	-	nC
Gate-Source Charge	Q_{gs}		-	11	-	nC
Gate-Drain Charge	Q_{gd}		-	10	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current	I_S		-	-	145	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F =20A di/dt = 100A/μs	-	44	-	nS
Reverse Recovery Charge	Qrr		-	40	-	nC

Notes:

1. EAS condition : Tj=25℃,V_{DD}=20V,V_G=10V,L=0.5mH,Rg=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

Typical Electrical and Thermal Characteristics

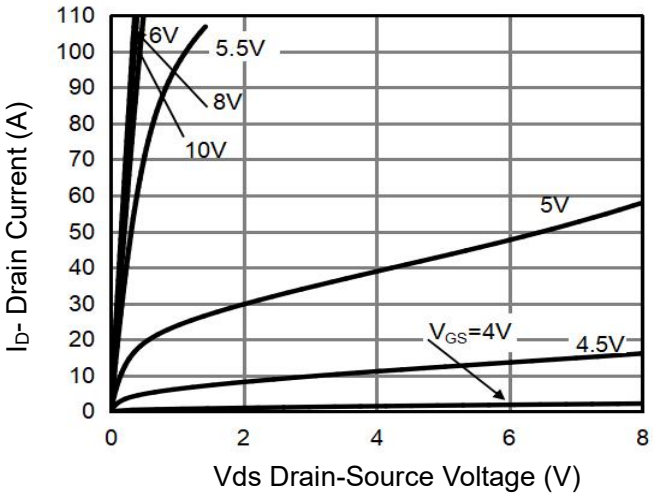


Figure 1 Output Characteristics

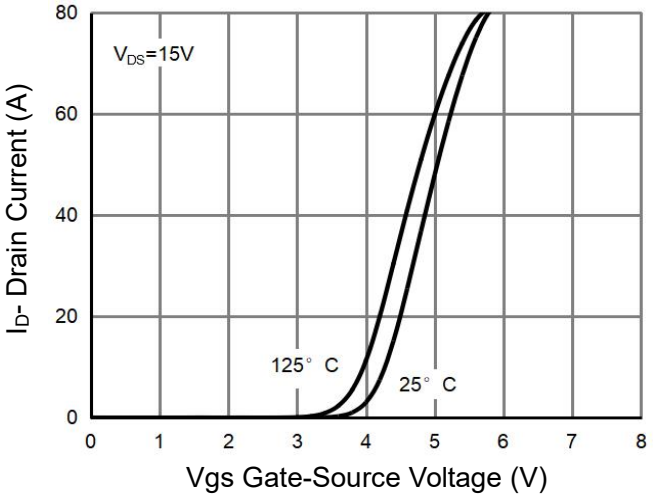


Figure 2 Transfer Characteristics

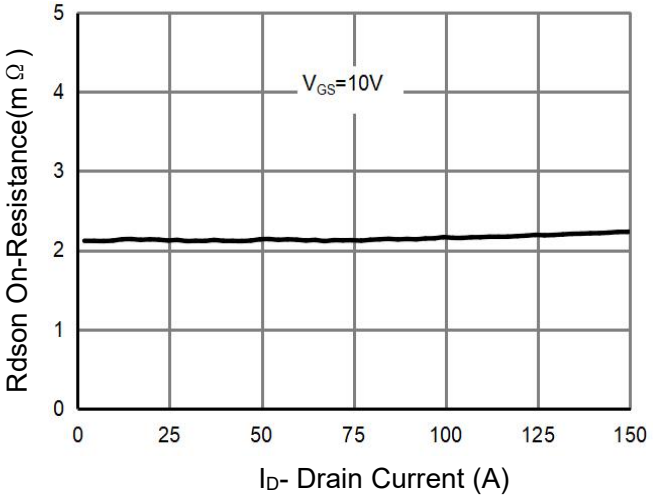


Figure 3 Rdson- Drain Current

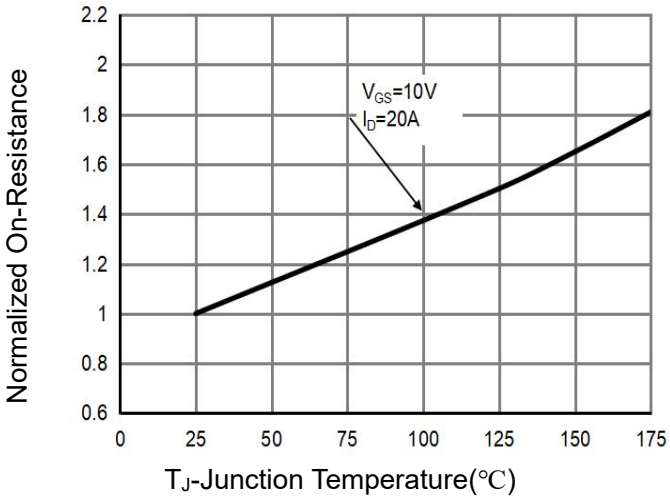


Figure 4 Rdson-Junction Temperature

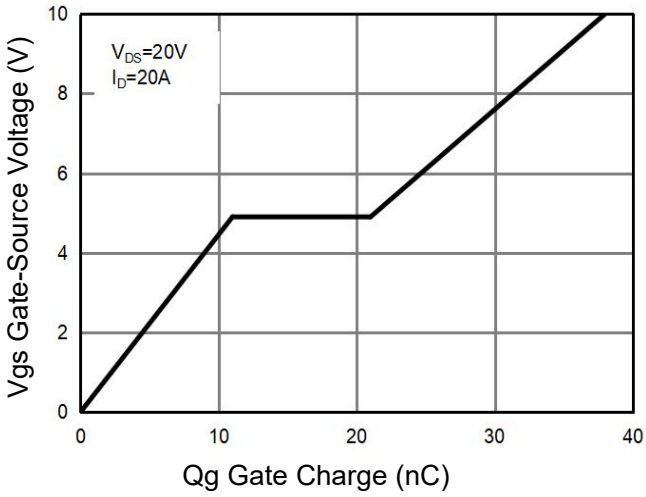


Figure 5 Gate Charge

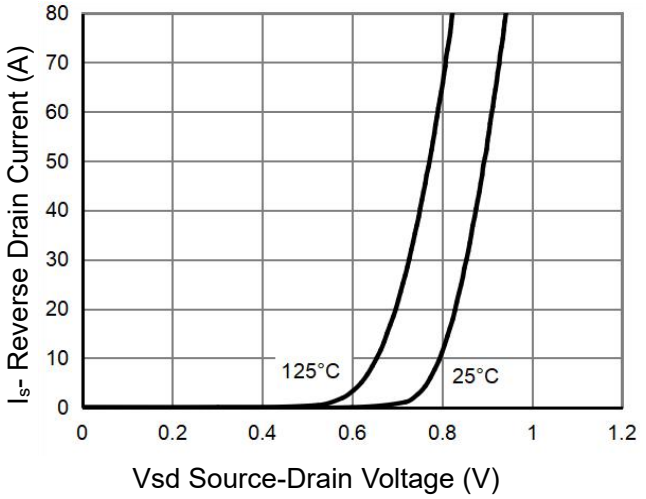


Figure 6 Source- Drain Diode Forward

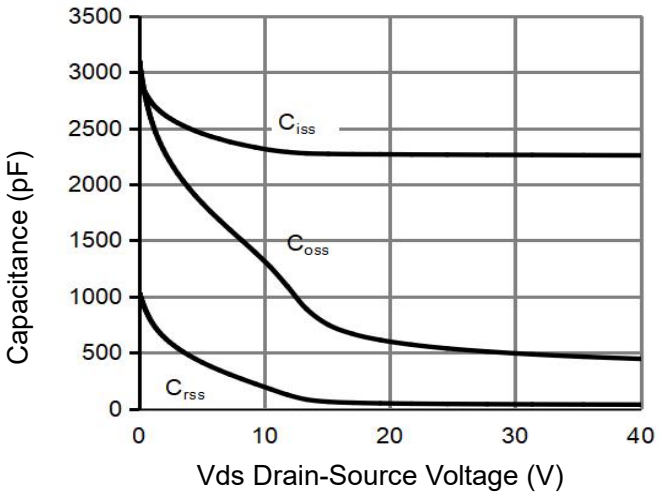


Figure 7 Capacitance vs Vds

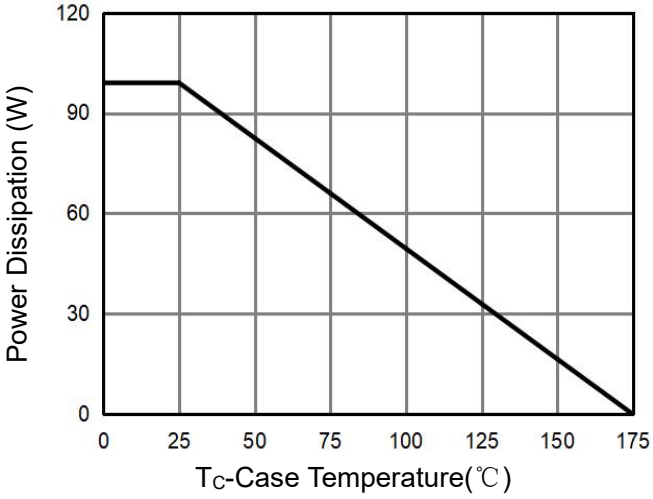


Figure 9 Power De-rating

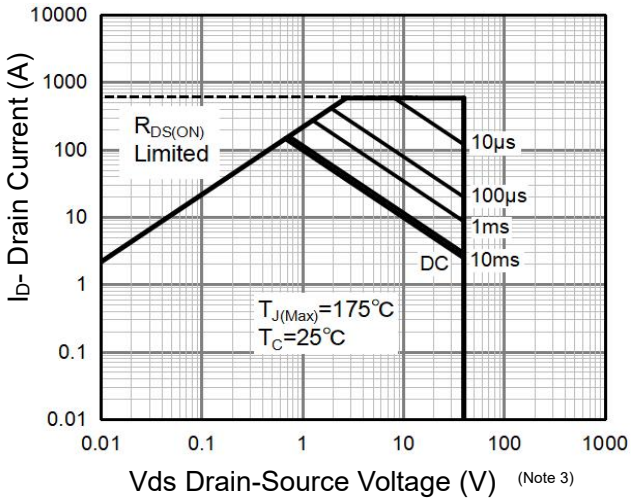


Figure 8 Safe Operation Area

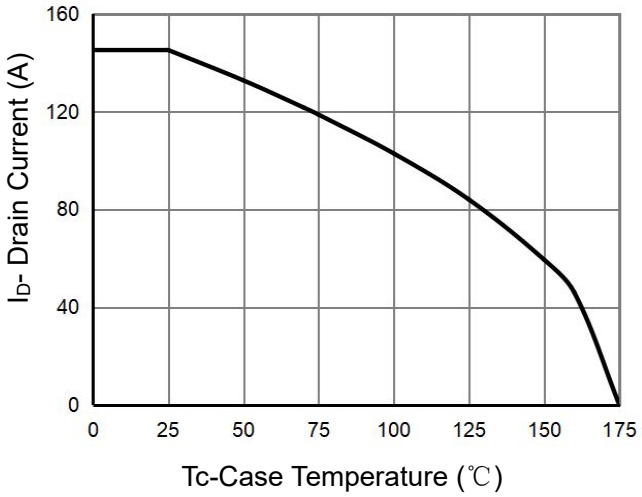


Figure 10 Current De-rating

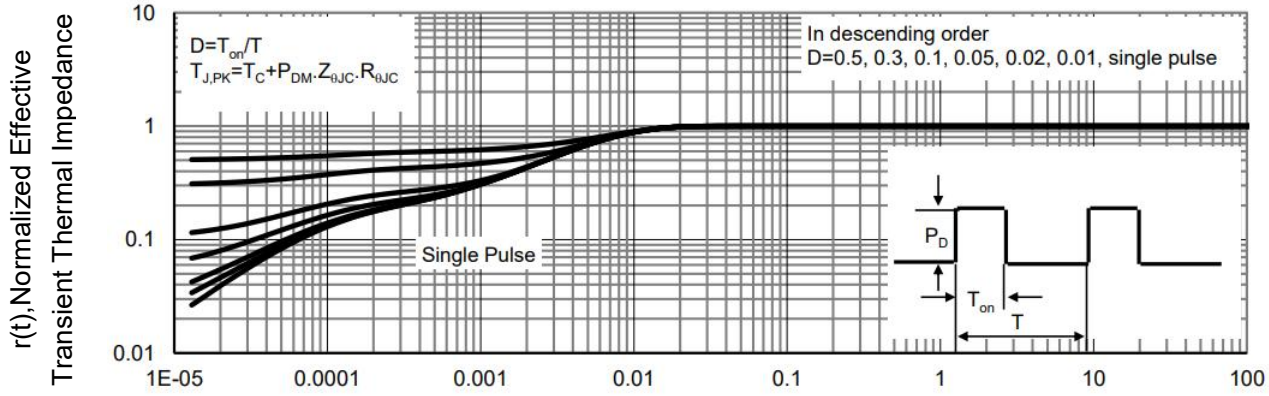
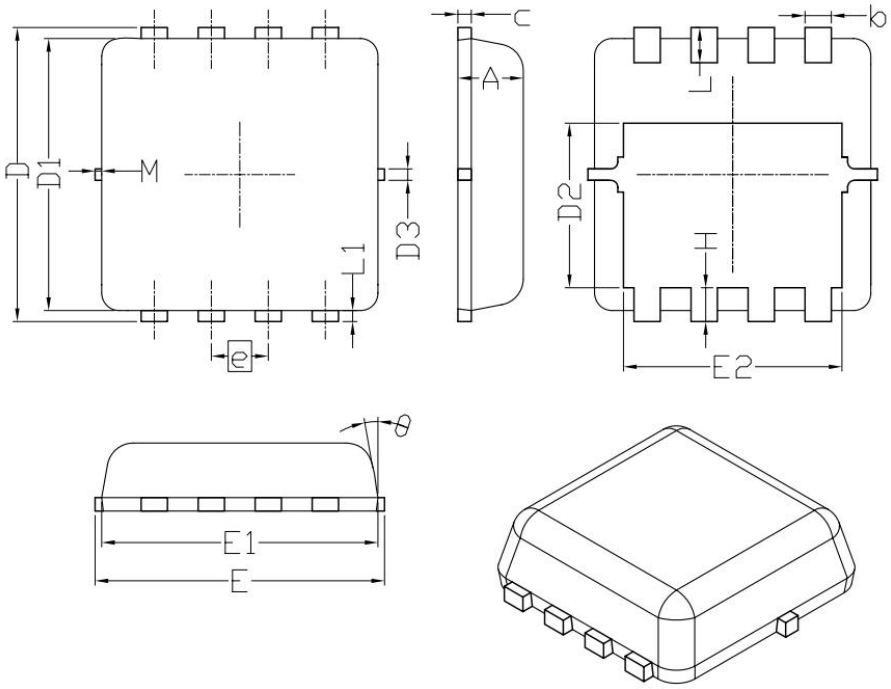
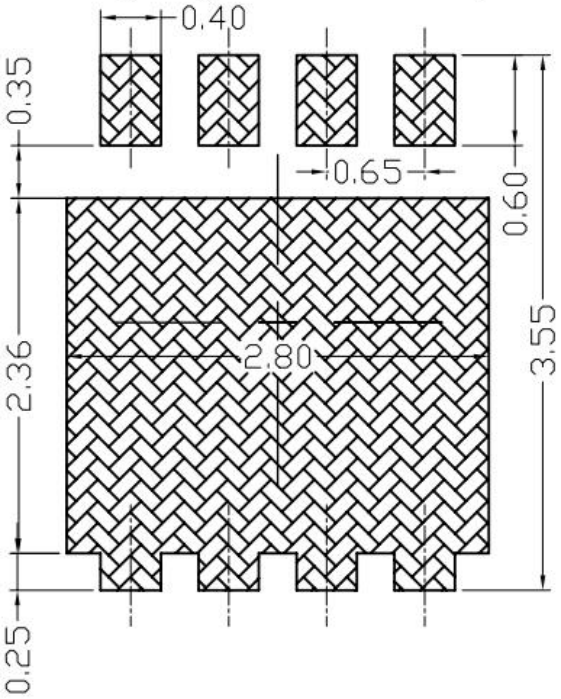


Figure 11 Normalized Maximum Transient Thermal Impedance

PDFN3.3X3.3-8L Package Information



Land Pattern
(Only for Reference)



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.10	3.20	3.30
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			

Revision History

Revision	Date	Subjects
V1.0	2025.08.27	Product data sheet

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