NCE N-Channel Super Trench III Power MOSFET

Description

The series of devices uses **Super Trench III** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

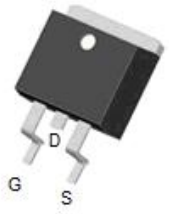
- V_{DS} =80V,I_D =319A
  $R_{DS(ON)}$=1.45mΩ , typical (TO-220)@ V_{GS}=10V
  $R_{DS(ON)}$=1.25mΩ , typical (TO-263)@ V_{GS}=10V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating

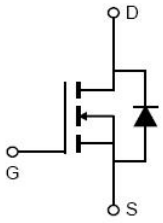
100% UIS TESTED!
100% ΔVds TESTED!

TO-220-3L



TO-263-2L





Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP018NH80	NCEP018NH80	TO-220-3L	-	-	-
NCEP018NH80D	NCEP018NH80D	TO-263-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	319	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	223	A
Pulsed Drain Current	I_{DM}	1276	A
Maximum Power Dissipation	P_D	340	W
Derating factor		2.27	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	2704	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.44	℃/W
Thermal Resistance,Junction-to-Ambient (Note 4)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA		80		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V		-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V		-	-	±100	nA
On Characteristics							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA		2.5	3.5	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	TO-220	-	1.45	1.8	mΩ
			TO-263		1.25	1.8	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A			90	-	S
Dynamic Characteristics							
Input Capacitance	C_{lss}	V_{DS}=40V,V_{GS}=0V, F=1.0MHz		-	11780	-	PF
Output Capacitance	C_{oss}			-	5800	-	PF
Reverse Transfer Capacitance	C_{rss}			-	161	-	PF
Switching Characteristics (Note 2)							
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=40V,I_D=20A V_{GS}=10V,R_G=3Ω		-	33.4	-	nS
Turn-on Rise Time	t_r			-	11.8	-	nS
Turn-Off Delay Time	$t_{d(off)}$			-	40.35	-	nS
Turn-Off Fall Time	t_f			-	10.2	-	nS
Total Gate Charge	Q_g	V_{DS}=40V,I_D=20A, V_{GS}=10V		-	168	-	nC
Gate-Source Charge	Q_{gs}			-	46		nC
Gate-Drain Charge	Q_{gd}			-	41.5		nC
Drain-Source Diode Characteristics							
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A		-		1.2	V
Diode Forward Current	I_S			-	-	319	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 20A di/dt = 100A/μs		-	84.5	-	nS
Reverse Recovery Charge	Qrr			-	163	-	nC

Notes:

1. EAS condition : Tj=25℃,V_{DD}=40V,V_G=10V,L=0.5mH,Rg=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design.

Typical Electrical and Thermal Characteristics

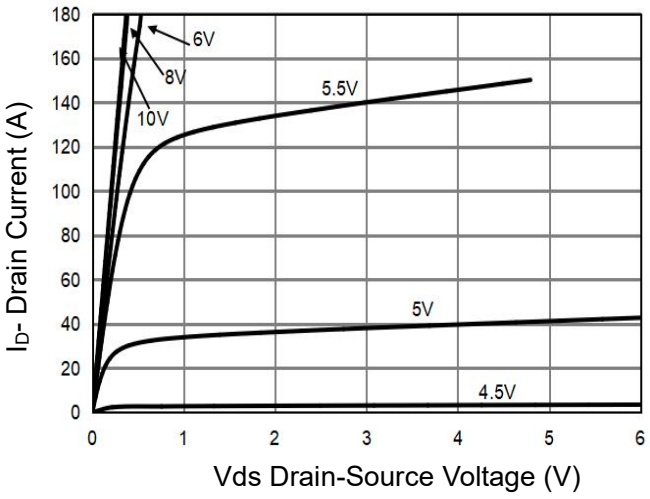


Figure 1 Output Characteristics

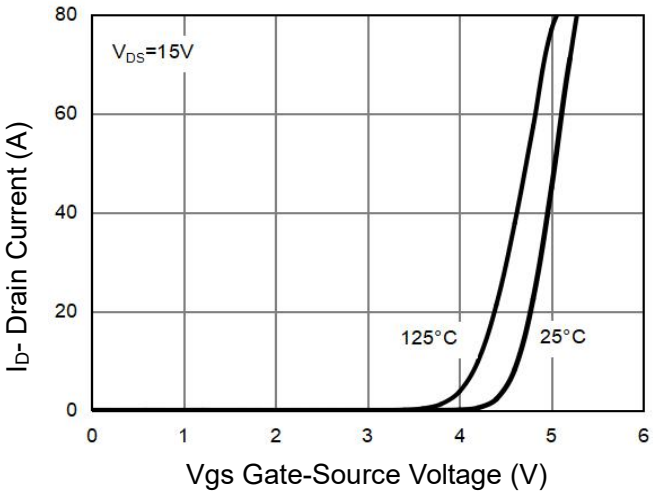


Figure 2 Transfer Characteristics

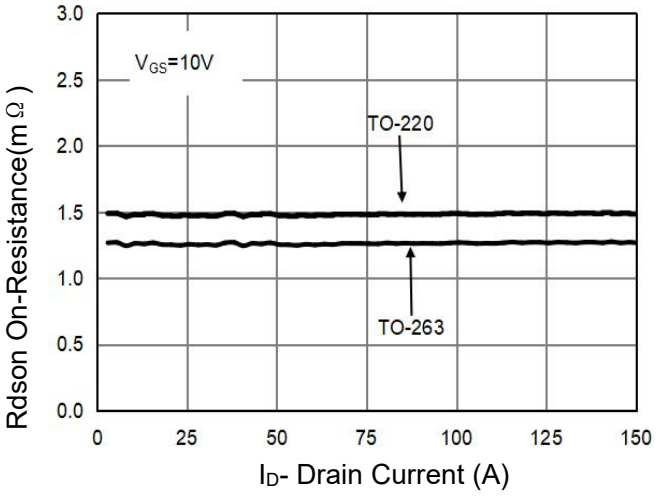


Figure 3 Rdson- Drain Current

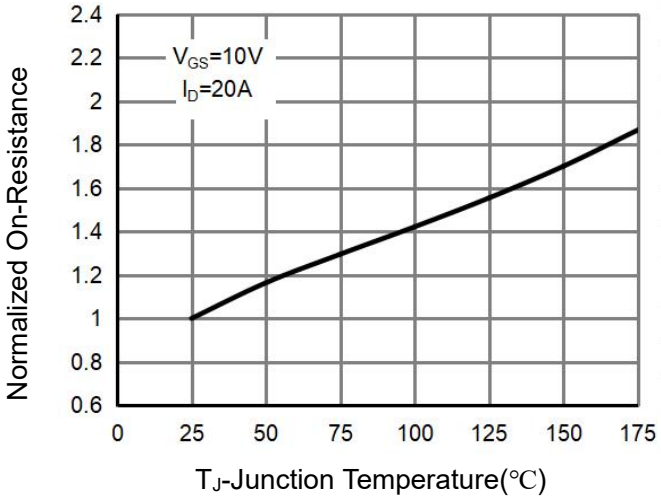


Figure 4 Rdson-Junction Temperature

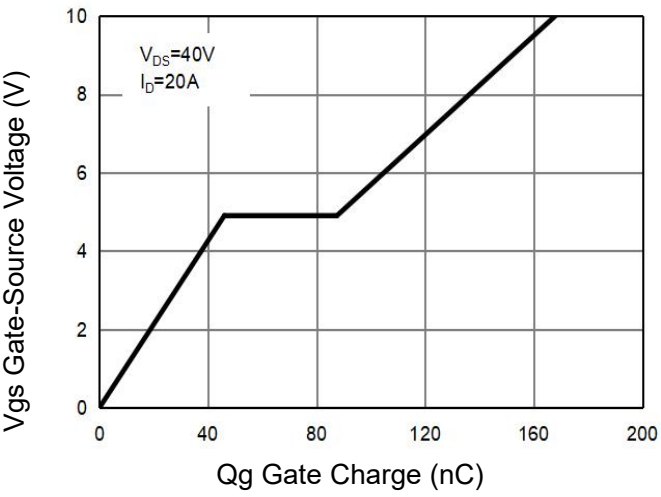


Figure 5 Gate Charge

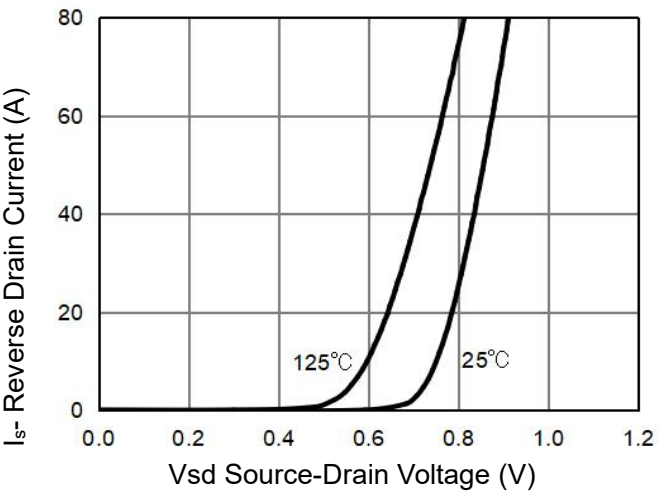


Figure 6 Source- Drain Diode Forward

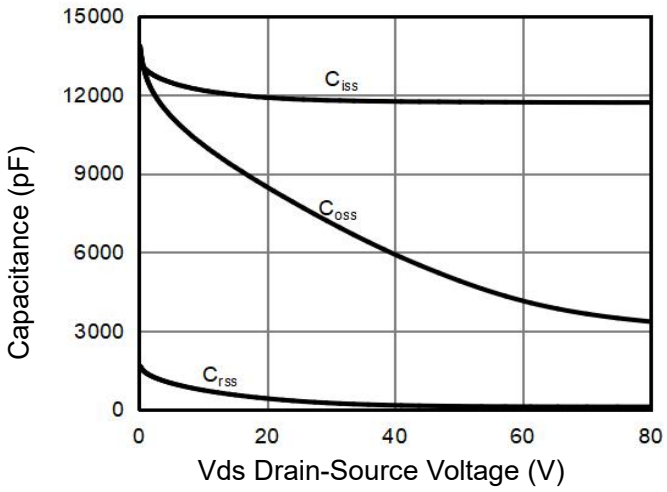


Figure 7 Capacitance vs Vds

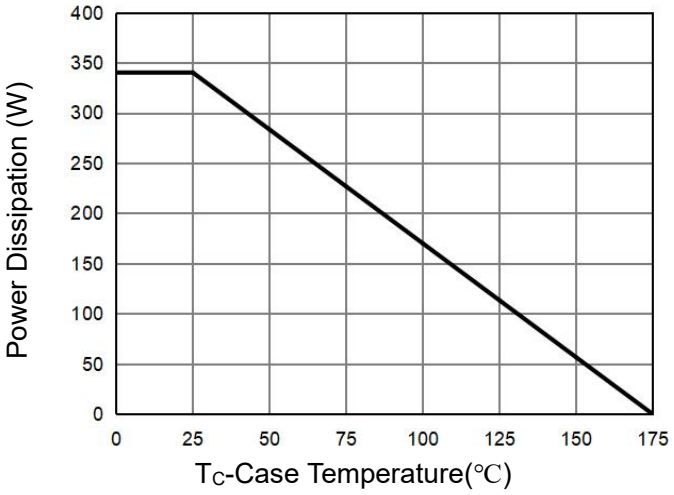


Figure 9 Power De-rating

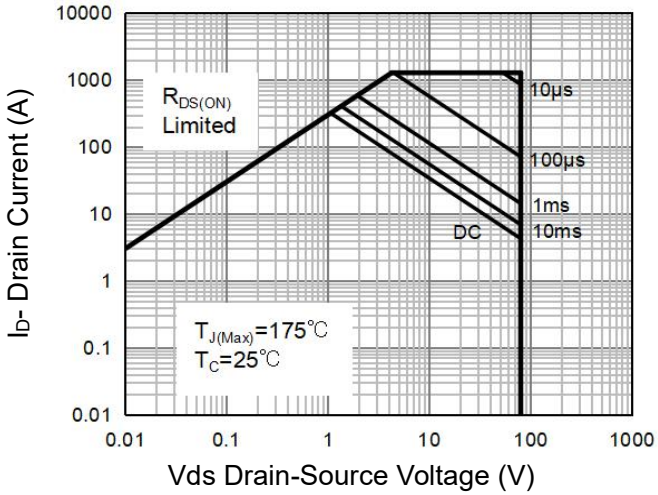


Figure 8 Safe Operation Area(Note 3)

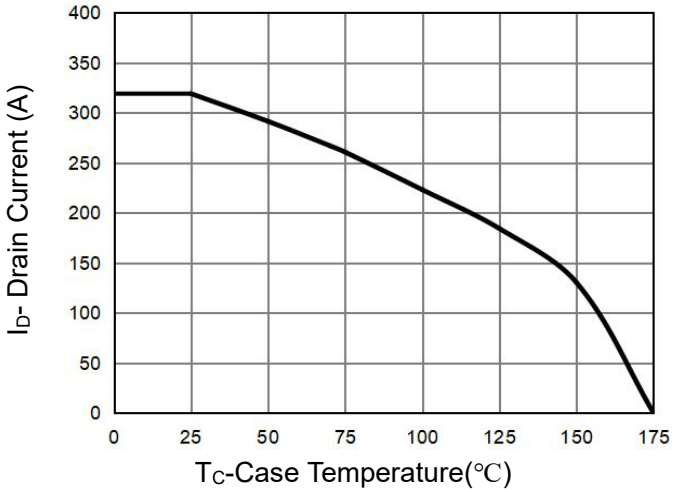


Figure 10 Current De-rating

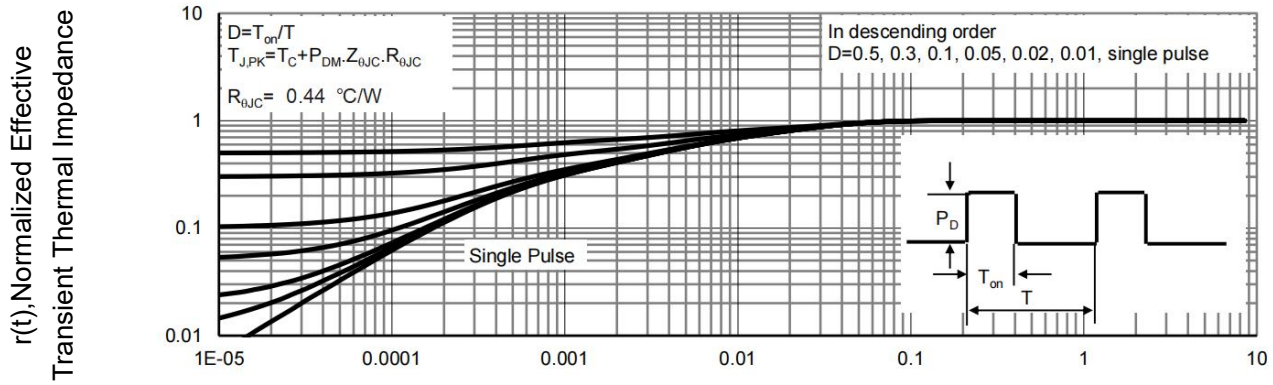
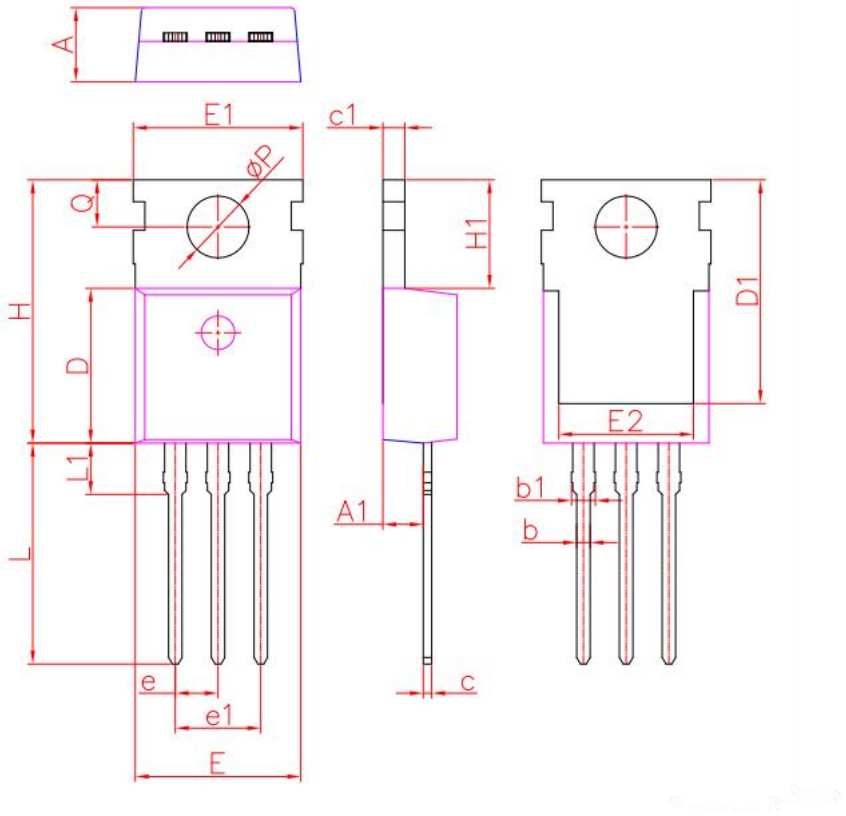


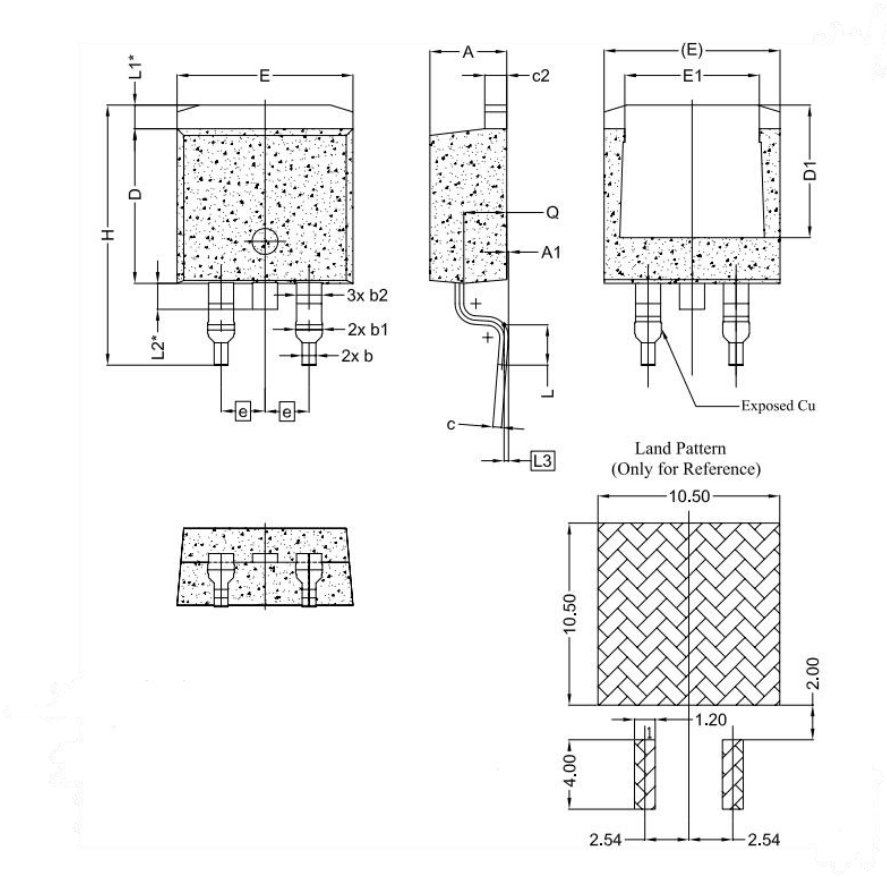
Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



TO220			
DIM.	MIN.	NOM.	MAX.
A	4.20	4.40	4.60
A1	2.25	2.40	2.55
b	0.70	0.80	0.90
b1	1.17	1.27	1.37
c	0.33	0.50	0.65
c1	1.20	1.30	1.40
D	8.95	9.20	9.75
D1	13.10	13.30	13.50
E	9.74	9.84	10.04
E1	9.91	10.08	10.25
E2	7.90	8.00	8.10
e	2.54BSC		
e1	5.08BSC		
H	15.45	15.65	15.85
H1	6.30	6.45	6.60
L	12.90	13.13	13.40
L1	2.85	3.05	3.25
Q	2.65	2.80	2.95
øP	3.40	3.68	3.80
All dimensions in millimeters			

TO-263-2L Package Information



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	4.24	4.44	4.64
A1	0.00	0.10	0.25
b	0.70	0.80	0.90
b1	1.20	1.55	1.75
b2	1.20	1.45	1.70
c	0.40	0.50	0.60
c2	1.15	1.27	1.40
D	8.82	8.92	9.02
D1	6.86	7.65	—
E	9.96	10.16	10.36
E1	6.89	7.77	7.89
e	2.54 BSC		
H	14.61	15.00	15.88
L	1.78	2.32	2.79
L1	1.36 REF.		
L2	1.50 REF.		
L3	0.25 BSC		
Q	2.30	2.48	2.70

Revision History

Revision	Date	Subjects
V1.0	2025.07.23	Product data sheet
V2.0	2025.07.31	Update $R_{\theta JC}$&P_D&I_D Update Figure 8 Safe Operation Area

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