NCE N-Channel Super Trench II Power MOSFET

Description

The series of devices uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

Application

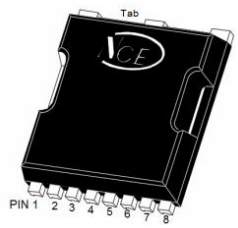
- High-frequency Switching and Synchronous Rectification
- DC/DC and AC/DC Converter
- Motor Driver
- Battery Management System (BMS)

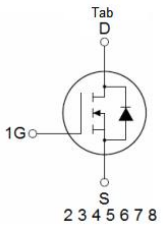
General Features

- V_{DS} =100V,I_D =273A
  $R_{DS(ON)}$=2.05mΩ , typical@ V_{GS}=10V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔVds TESTED!

TOLL-8L





Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP025N10MLL	NCEP025N10MLL	TOLL-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	273	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	191	A
Pulsed Drain Current	I_{DM}	1092	A
Maximum Power Dissipation	P_D	355	W
Derating factor		2.37	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	1731	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.42	℃/W
Thermal Resistance,Junction-to-Ambient (Note4)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-	2.05	2.50	mΩ
Gate resistance	R_G	V_{GS}=0V,V_{DS}=0V,F=1.0MHz	-	1.3	-	Ω
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=40A	-	100	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz	-	15180	-	pF
Output Capacitance	C_{oss}		-	1100	-	pF
Reverse Transfer Capacitance	C_{rss}		-	82	-	pF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V,I_D=40A V_{GS}=10V,R_G=1.6Ω	-	41.8	-	nS
Turn-on Rise Time	t_r		-	58.9	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	148.4	-	nS
Turn-Off Fall Time	t_f		-	48.6	-	nS
Total Gate Charge	Q_g	V_{DS}=50V,I_D=20A, V_{GS}=10V	-	212	-	nC
Gate-Source Charge	Q_{gs}		-	62	-	nC
Gate-Drain Charge	Q_{gd}		-	50	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=40A	-	-	1.2	V
Diode Forward Current	I_S		-	-	273	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 40A di/dt = 100A/μs	-	67	-	nS
Reverse Recovery Charge	Qrr		-	149	-	nC

Notes:

1. EAS condition : Tj=25℃,VDD=50V,VG=10V,L=0.5mH,Rg=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of TJ(MAX)=175°C. The SOA curve provides a single pulse rating.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board desi

Typical Electrical and Thermal Characteristics

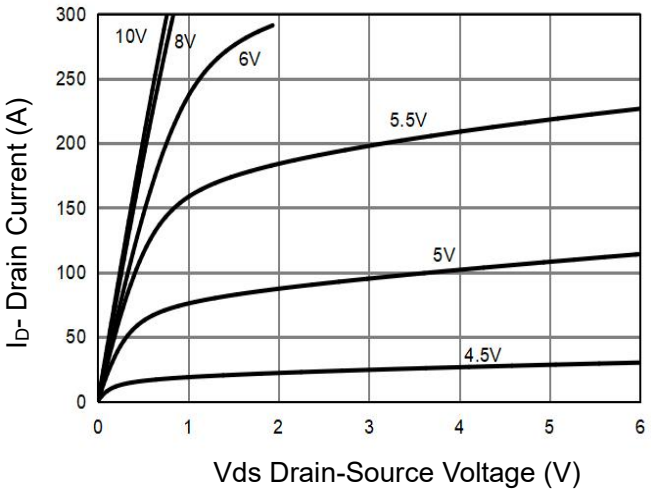


Figure 1 Output Characteristics

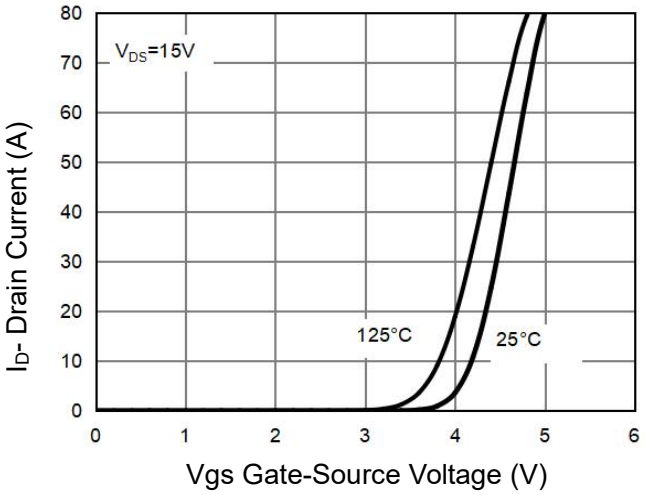


Figure 2 Transfer Characteristics

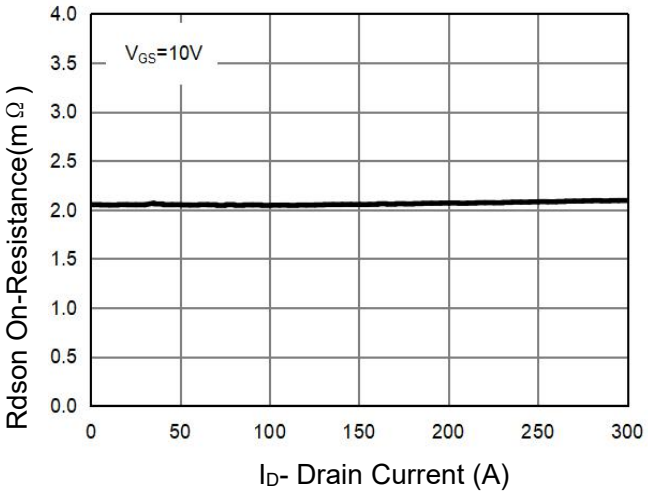


Figure 3 Rdson- Drain Current

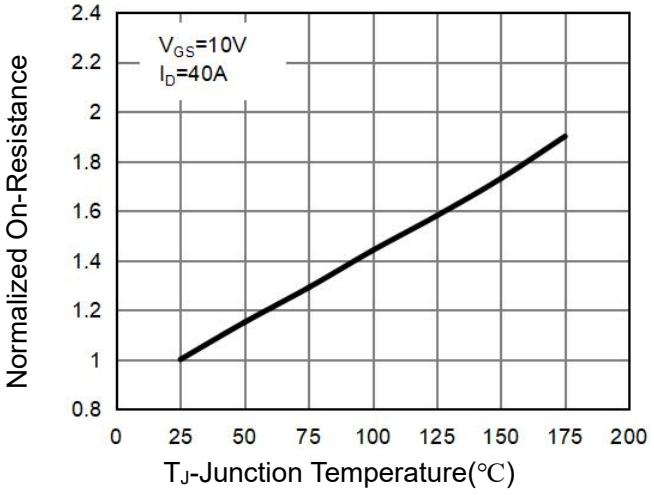


Figure 4 Rdson-Junction Temperature

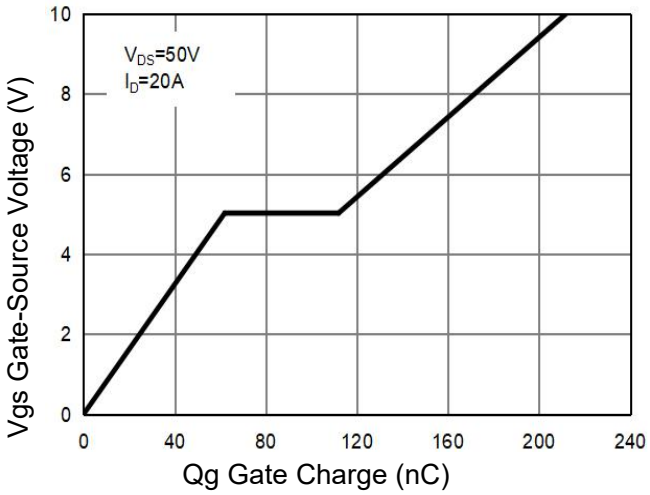


Figure 5 Gate Charge

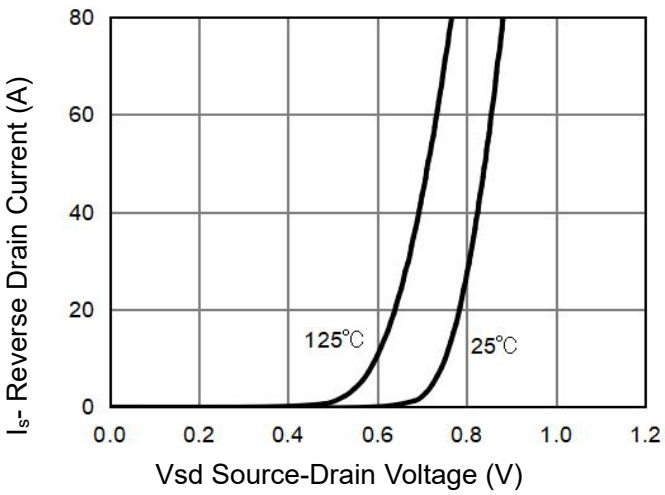


Figure 6 Source- Drain Diode Forward

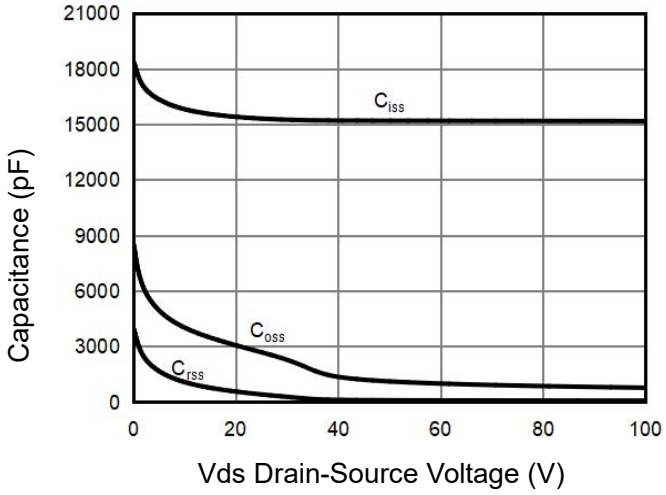


Figure 7 Capacitance vs Vds

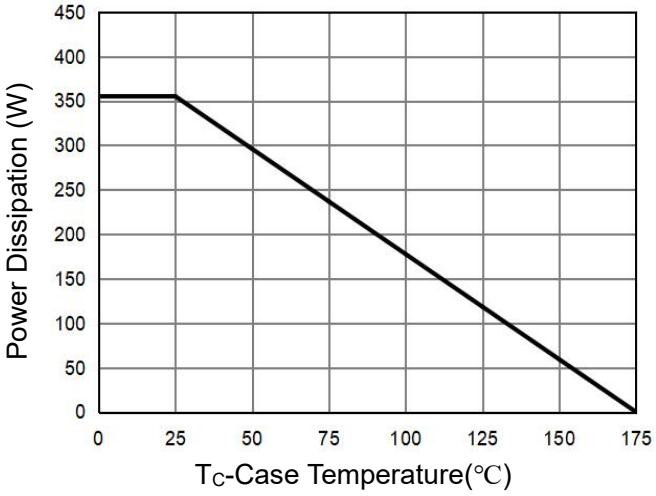


Figure 9 Power De-rating

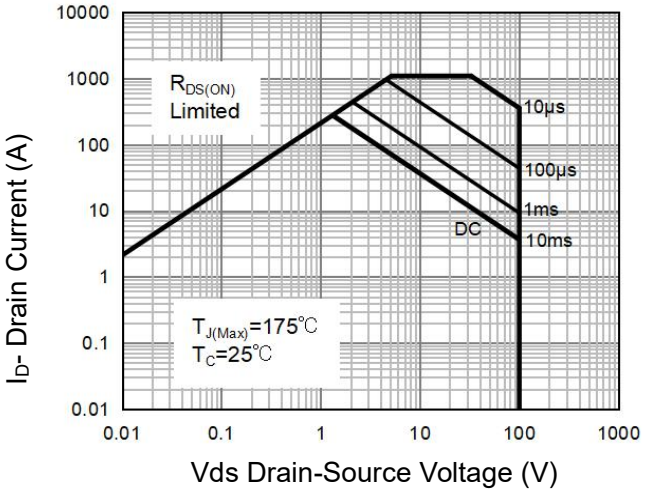


Figure 8 Safe Operation Area (Note3)

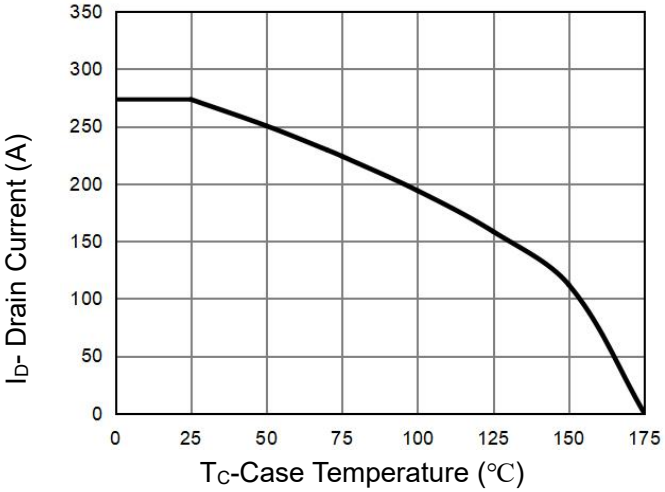


Figure 10 Current De-rating

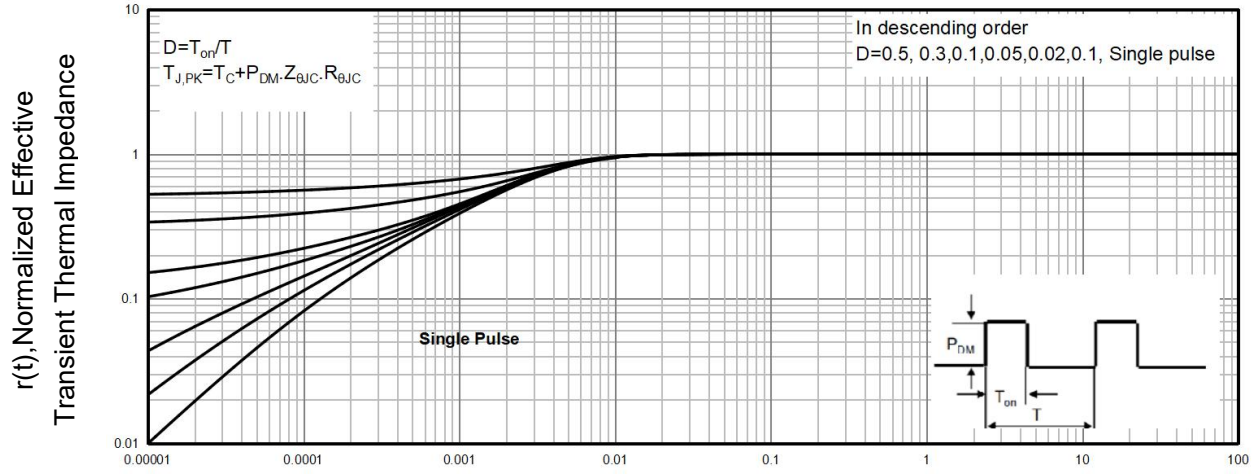
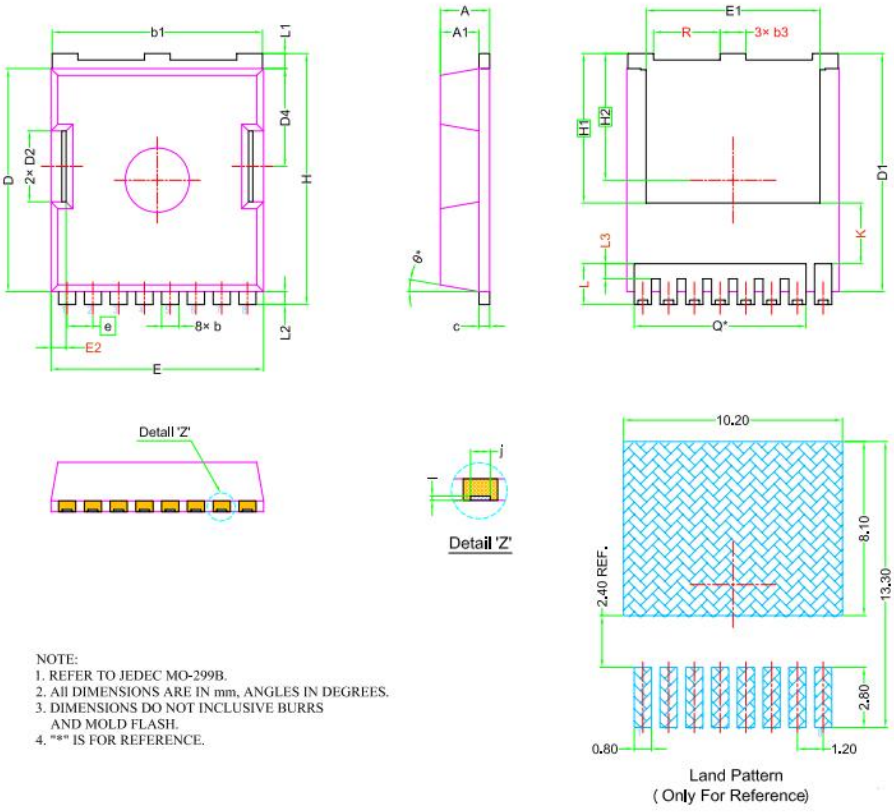


Figure 11 Normalized Maximum Transient Thermal Impedance

TOLL-8L Package Information



NOTE:
1. REFER TO JEDEC MO-299B.
2. All DIMENSIONS ARE IN mm, ANGLES IN DEGREES.
3. DIMENSIONS DO NOT INCLUSIVE BURRS AND MOLD FLASH.
4. "*" IS FOR REFERENCE.

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D4	4.45	4.55	4.65
E	9.80	9.90	10.00
E1	8.00	8.10	8.20
E2	0.60	0.70	0.80
e	1.20 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
H2	5.89 BSC		
i	0.10 REF.		
j	0.46 REF.		
K	2.80 REF.		
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.30	0.70	0.80
N	8		
Q	8.00 REF.		
R	3.00	3.10	3.20
θ	10° REF.		

Revision History

Revision	Date	Subjects
V1.0	2026.04.17	Product data sheet

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