NCE N-Channel Super Trench II Power MOSFET

Description

The series of devices uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

Application

- High-frequency Switching and Synchronous Rectification
- DC/DC and AC/DC Converter
- Motor Driver
- Battery Management System (BMS)

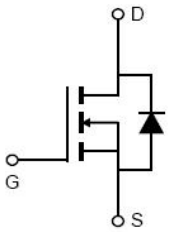
General Features

- V_{DS} =200V,I_D =115A
  $R_{DS(ON)}$=9.3mΩ , typical @ V_{GS}=10V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- Optimized body diode reverse recovery performance

100% UIS TESTED!
100% ΔVds TESTED!

TO-220-3L





Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP090NS20	NCEP090NS20	TO-220-3L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	115	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	81	A
Pulsed Drain Current	I_{DM}	460	A
Maximum Power Dissipation	P_D	340	W
Derating factor		2.27	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	1692	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.44	℃/W
Thermal Resistance,Junction-to-Ambient (Note 4)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	200	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	9.3	10.7	mΩ
Gate resistance	R_G	V_{GS}=0V,V_{DS}=0V,F=1.0MHz	-	1.6	-	Ω
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A	60	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=100V,V_{GS}=0V, F=1.0MHz	-	6000	-	PF
Output Capacitance	C_{oss}		-	535	-	PF
Reverse Transfer Capacitance	C_{rss}		-	17.5	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=100V,I_D=20A V_{GS}=10V,R_G=4.7Ω	-	54	-	nS
Turn-on Rise Time	t_r		-	38	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	65	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	V_{DS}=100V,I_D=20A, V_{GS}=10V	-	95	-	nC
Gate-Source Charge	Q_{gs}		-	30.5	-	nC
Gate-Drain Charge	Q_{gd}		-	24.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current	I_S		-	-	115	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 20A di/dt = 100A/μs	-	70	-	nS
Reverse Recovery Charge	Qrr		-	130	-	nC

Notes:

1. EAS condition : Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heat sink, assuming a maximum junction temperature of TJ(MAX)=175° C. The SOA curve provides a single pulse rating.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design.

Typical Electrical and Thermal Characteristics

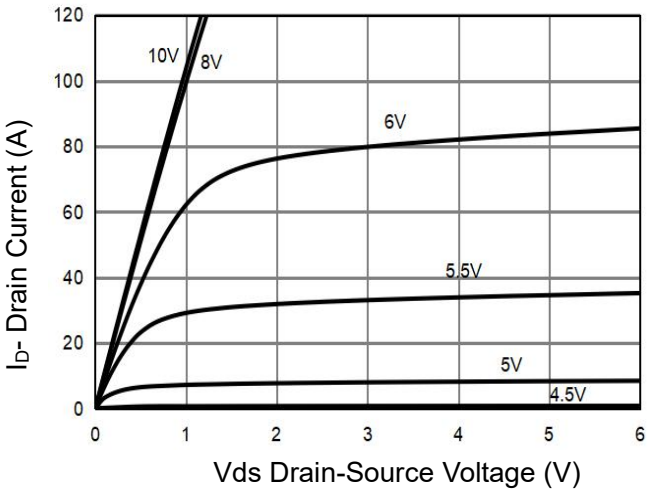


Figure 1 Output Characteristics

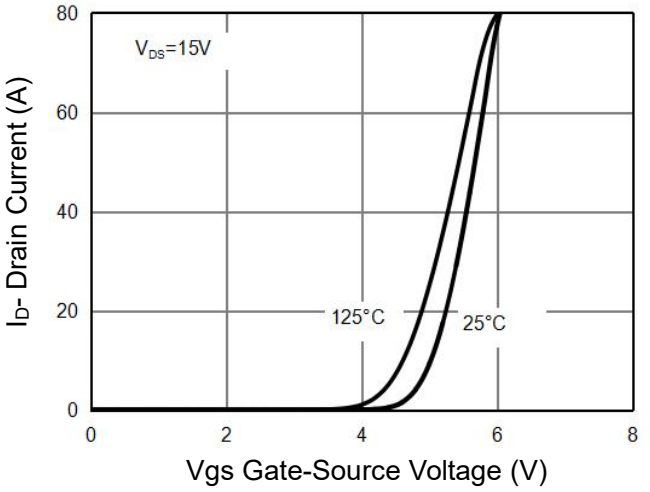


Figure 2 Transfer Characteristics

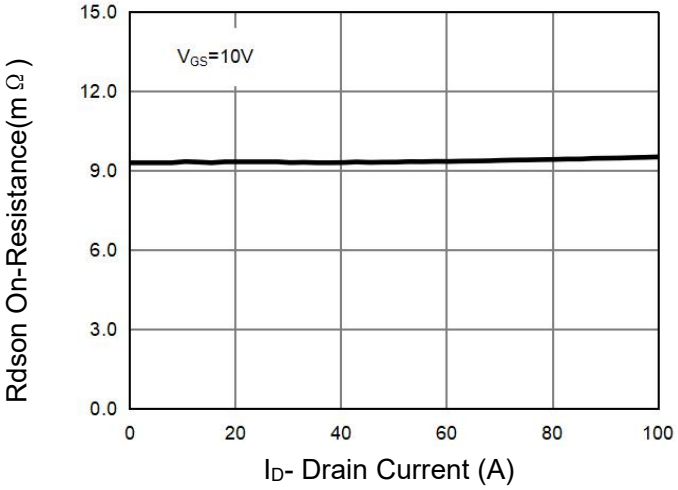


Figure 3 Rdson- Drain Current

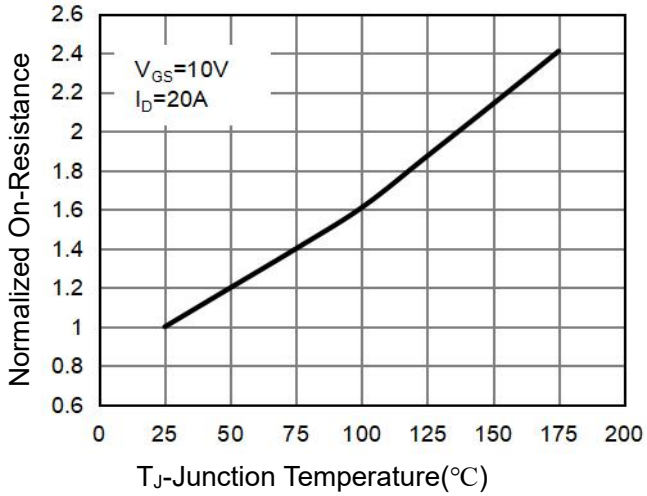


Figure 4 Rdson-JunctionTemperature

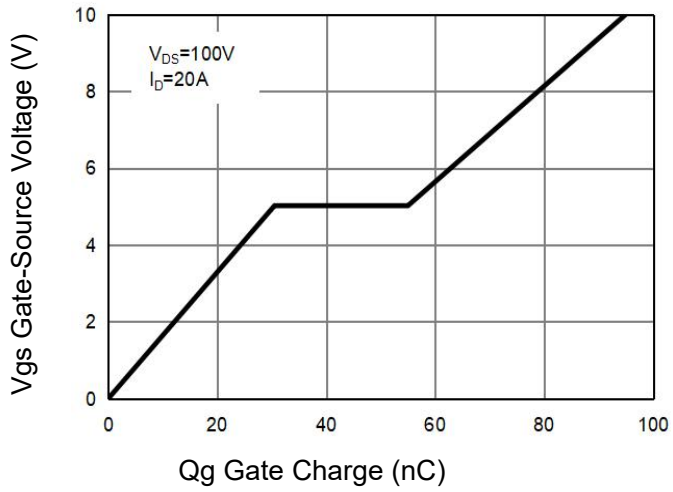


Figure 5 Gate Charge

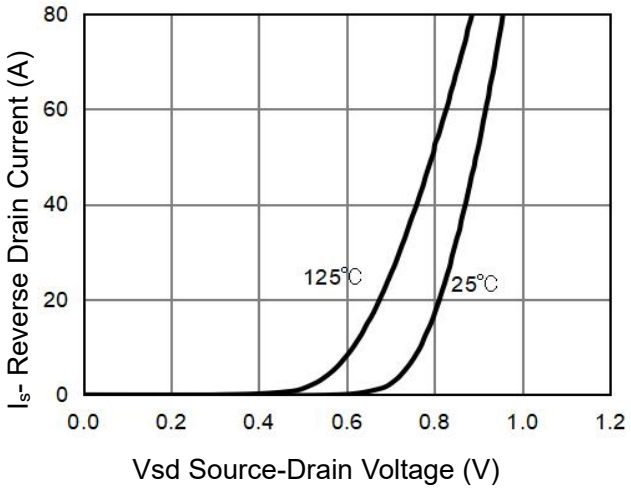


Figure 6 Source- Drain Diode Forward

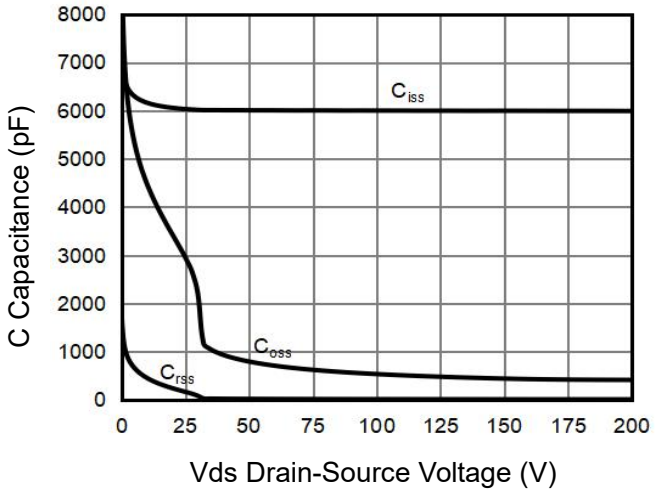


Figure 7 Capacitance vs Vds

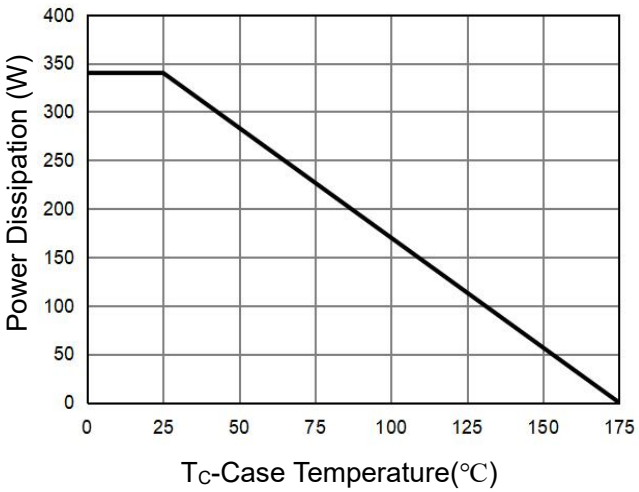


Figure 9 Power De-rating

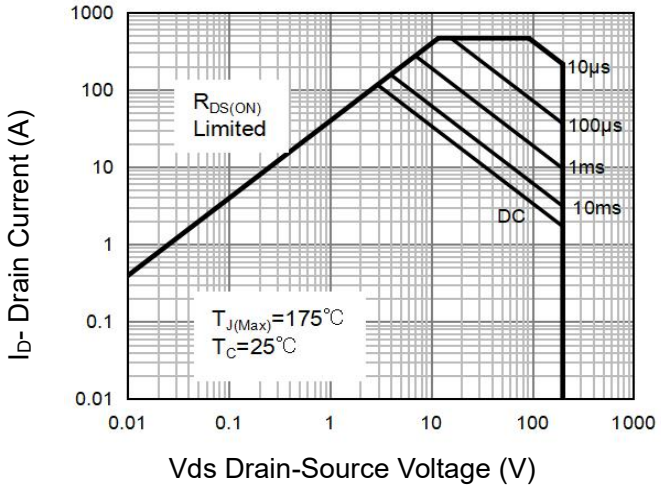


Figure 8 Safe Operation Area (Note3)

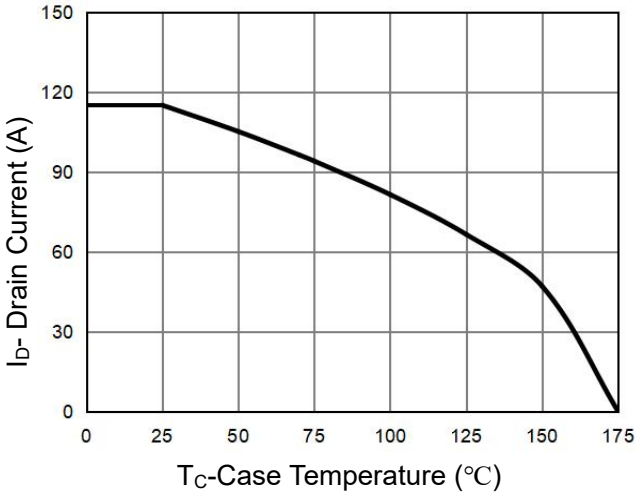


Figure 10 Current De-rating

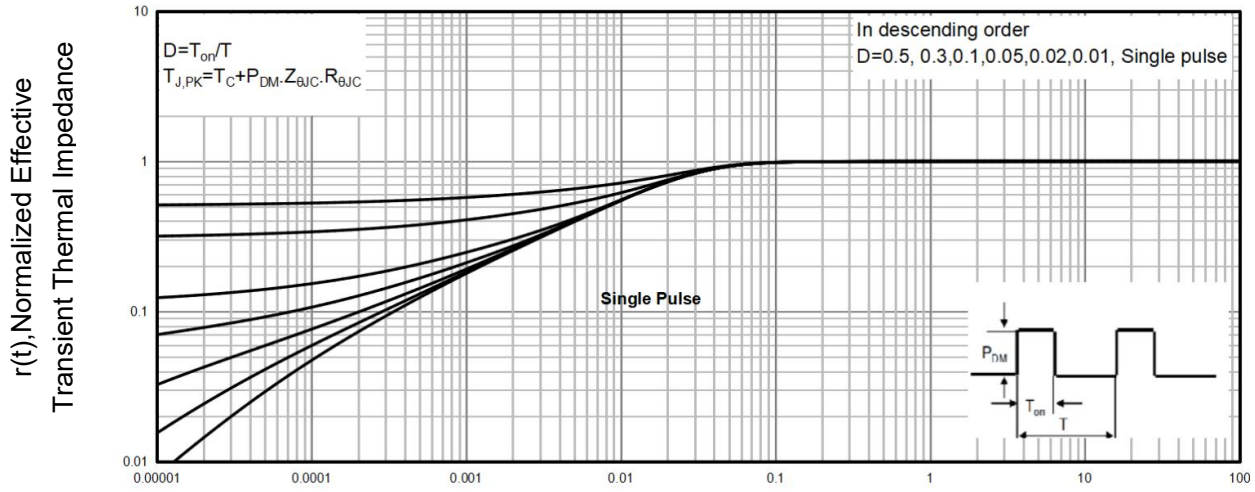
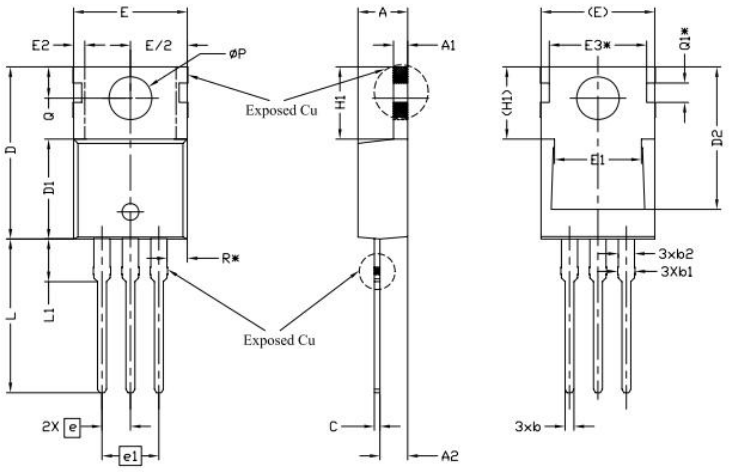


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information





Note:
1. Package Reference: JEDEC TO220, Variation AB.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimensions E, H1, D2 & E1.
6. Dimension E2 & H1 Define A Zone Where Stamping And Singulation Irregularities Are Allowed.
7. "*" is reference .

SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.24	4.44	4.64	
A1	1.15	1.27	1.40	
A2	2.30	2.48	2.70	
b	0.70	0.80	0.90	
b1	1.20	1.55	1.75	
b2	1.20	1.45	1.70	
c	0.40	0.50	0.60	
D	14.70	15.37	16.00	4
D1	8.82	8.92	9.02	
D2	12.43	12.73	12.83	5
E	9.96	10.16	10.36	4,5
E1	6.86	7.77	8.89	5
E2	-	-	0.76	6
E3*	8.70REF.			
e	2.54BSC			
e1	5.08BSC			
H1	6.30	6.45	6.60	5,6
L	13.47	13.72	13.97	
L1	3.60	3.80	4.00	
øP	3.75	3.84	3.93	
Q	2.60	2.80	3.00	
Q1*	1.73REF.			
R*	1.82REF.			

Revision History

Revision	Date	Subjects
V1.0	2026.09.16	Product data sheet

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